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OM  
/

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PM 1 (B)

ECE

ACE ACADEMY

VLSI

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## ① JFET:

→ Book: Microelectronics CKTs by Sedra & Smith (old edition).

- Construction and operation of JFET.
- Drain Char. & Transfer Characteristics.
- JFET biasing.
- Amplifiers Analysis.
- Frequency Analysis.

Book

Boyle sted.

## ② MOSFET:

→ Book: → CMOS VLSI Design by Weste & Harris (Ch. 1, 2 & 4).

→ Design of Analog CMOS IC by RAZAVI (Ch: 2 & 3)

- Depletion & Enhancement MOSFET.
- Construction & operation of MOSFET.
- Drain Char. & Transfer Characteristics.
- MOS Capacitor. ⊕ ✓
- MOSFET Analysis.
- Amplifier Analysis.
- Frequency Analysis. ⊕ ✓

## ③ CMOS:

- Implementation of functions in CMOS Technology. ✓

- Transfer Char. of cm Inverter. ✓
- Transistor sizing.
- Rise time, fall time, propagation Delay & Contamination Delay.
- Delay calculation.
- Power
- Noise Margin.

#### ④ Device Technology:

- IC fabrication technology:

##### Steps:

- ① oxidation.
  - ② Diffusion.
  - ③ Ion - implantation.
  - ④ Photolithography.
- n-tube (or) n-well.
  - p-tube (or) p-well.
  - Twin-tube (or) Double-well CMOS process.

# ★ Energy Band in Si (silicon):

2)

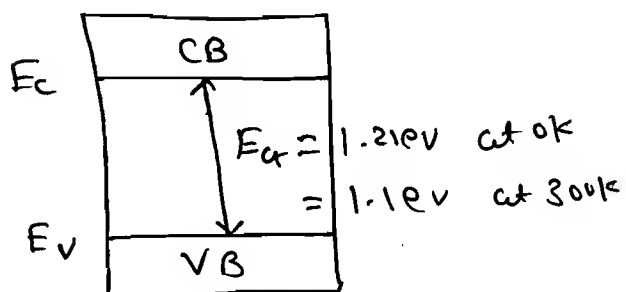
IMP

Concept: Why silicon (Si)?

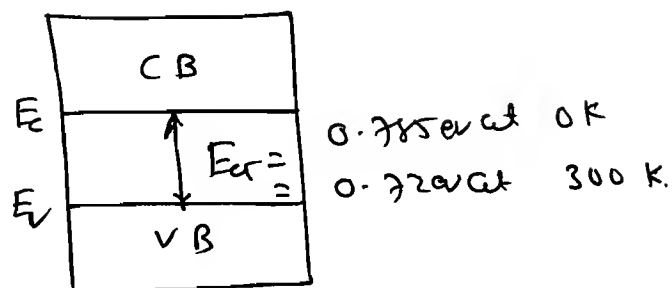
Ans: • Low leakage current.

$$\left. \begin{array}{l} I_0(\text{Si}) : \text{nA} \\ I_0(\text{Ge}) : \mu\text{A} \end{array} \right\} I_0(\text{Ge}) \approx 1000 I_0(\text{Si}).$$

• More energy gap.



Si



Ge

→ Carrier Concentration remain same for applied electric energy, it change only when thermal energy is applied.

• More Resistivity.

$$\rho_i(\text{Ge}) = 44.6 \approx 45 \Omega\text{-cm}$$

$$\rho_i(\text{Si}) = 231.5 \text{ K} \approx 230 \text{ K } \Omega\text{-cm}.$$

$$\rho_i = \frac{1}{n_i(\mu_p + \mu_n) \tau}$$

Si:  $\mu_n = \frac{\text{millman}}{1300} \text{ cm}^2/\text{V-s}$

$\mu_p = \frac{450}{500} \text{ cm}^2/\text{V-s}$

$n_i = 1.5 \times 10^{10} / \text{cm}^3.$

$\mu_n = 1350 \text{ cm}^2/\text{V-s}.$

$\mu_p = 480 \text{ cm}^2/\text{V-s}.$

Cre: millman

$$\mu_n = 3800 \text{ cm}^2/\text{V-s.}$$

$$\mu_p = 1800 \text{ cm}^2/\text{V-s.}$$

SMJ

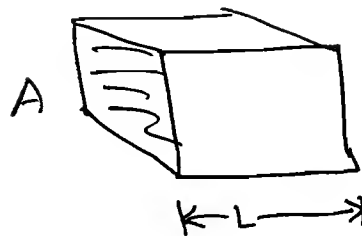
$$\mu_n = 3900 \text{ cm}^2/\text{V-s.}$$

$$\mu_p = 1900 \text{ cm}^2/\text{V-s.}$$

• More Resistance:

$$R_{(si)} = \frac{\rho_{(si)} L}{A}$$

$$R_{(cre)} = \frac{\rho_{(cre)} L}{A}$$



A & L same for the both.

$$R_{(si)} > R_{(cre)}.$$

So, more electron attenuation in si. So,  
Low leakage current in si.

- High Temp. (withstand).

$$\text{Si} \rightarrow 1425^\circ\text{C}$$

$$\text{Cre} \rightarrow 938^\circ\text{C.}$$

- High Voltage (sustained).

→ VLSI stands for very large scale integration.

→ This is a field which involves integration (or) packing more & more devices in a smaller and smaller area.

3)  
⇒ All RF devices are made up of

Gallium Arsenide (GaAs)

GaAs:  $\mu_n = 8500 \text{ cm}^2/\text{V.s.}$

$\mu_p = 400 \text{ cm}^2/\text{V.s.}$

→ Ga has high mobility for high current & high freq.

→ si for Low and medium freq.

→ npn is used instead of pnp because high mobility of electron in npn compared to pnp.

→ Bardeen, Brattain & Shockley was invented first transistor in 1948.

→ Schockley invented FET in 1952

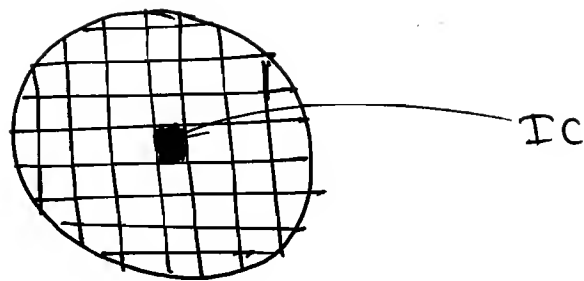
→ Jack Kilby invented IC in 1958.

→ Kahng & Atalla invented MOSFET in 1960.

→ Integrated circuit consist of active & passive devices & also interconnection in a integrated (or) package on a single crystal of a si chip.

→ IC fabrication is a ~~batch~~ batch process that is more no. of CKTs & IC's can be fabricated at one go.

⇒



Wafer (100 to 800 IC's)

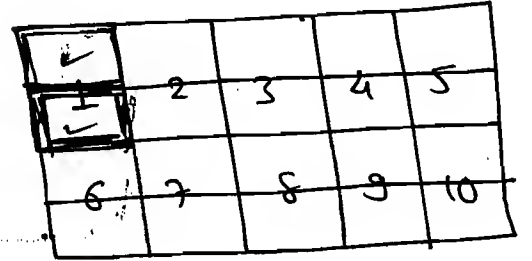
### \* Advantages of IC:

- Smaller size.
- Cost → Low
- Low Power
- High Speed
- Reliable
- Better performance.
- miniaturization & hence increase the equipment density.
- Cost reduction due to batch processing.
- Increase Reliability due to elimination of soldering joints.
- Improved function of performance i.e. Complex circuitry can be fabricated with better characteristics.
- Increase operating speeds due to reduction of parasitics.
- Reduction in power consumption.



→ In 1965 Gordon Moore (founder of Intel) observed that transistor count becomes double for every 18 to 24 months.

$$\rightarrow \frac{\text{Size}}{2} \Rightarrow \frac{\text{Area}}{2} = \frac{W \times L}{\sqrt{2} \sqrt{2}}$$



Scaling factor  
(s or d) =  $\sqrt{2}$ .

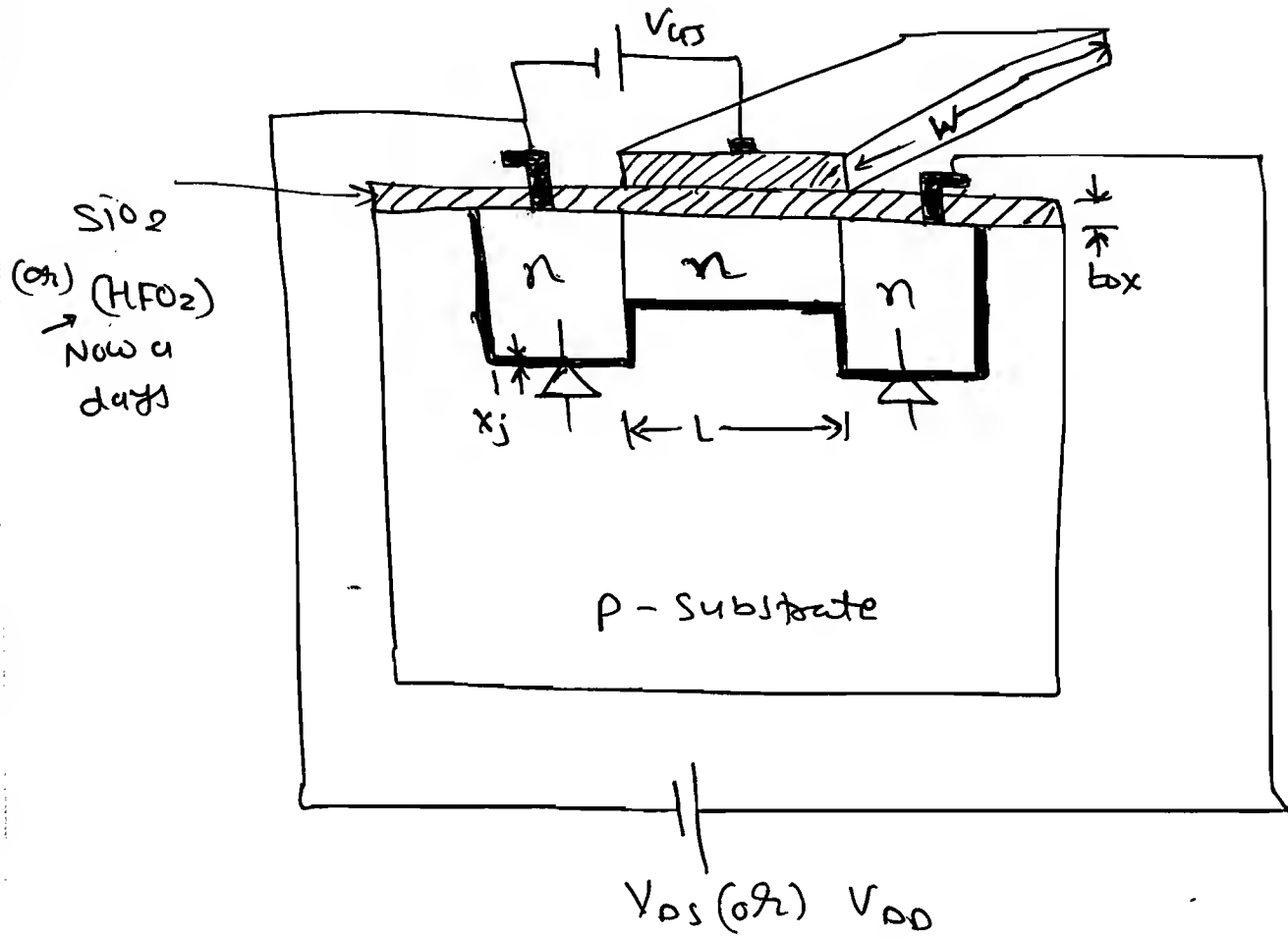
* Technology	Scaling:-	(in terms of channel length): L
L = 10 $\mu\text{m}$	10 $\mu\text{m}$	180 nm
(4004 $\mu\text{P}$ )	6 $\mu\text{m}$	130 nm
1971	3 $\mu\text{m}$	90 nm
	1.5 $\mu\text{m}$	65 nm
	1 $\mu\text{m}$	45 nm
	0.8 $\mu\text{m}$	32 nm ✓
	0.6 $\mu\text{m}$	22 nm ✓
	0.35 $\mu\text{m}$	14 nm ✓
	0.25 $\mu\text{m}$	

now  
a days.

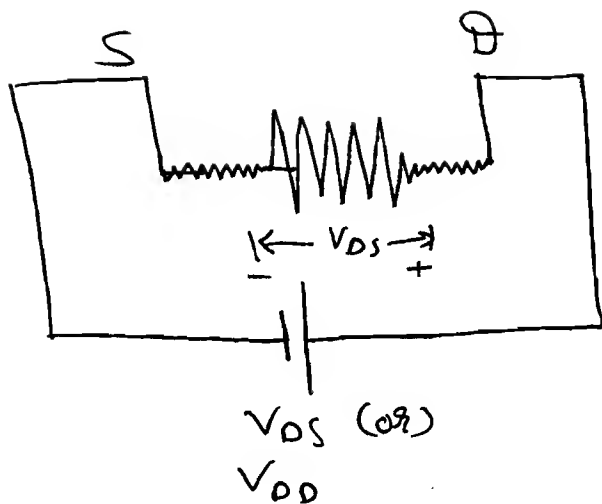
→ Channel length ( $\uparrow$ ) = Leakage Current  
( $\downarrow$ ) (Power) ( $\downarrow$ ).

## \* Scaling:

- ① Constant Field Scaling.
- ② Constant Voltage scaling.



- $L$  = Channel length.
- $W$  = Channel width.
- $t_{ox}$  = Gate oxide thickness.
- $x_j$  =  $n^+$  depletion thickness.
- $V_T$  = Threshold Voltage.
- $V_{DD}$  = power supply voltage.
- $N_A$  (or)  $N_D$  = Substrate Doping Concentration. (or) density.



$$E = \frac{V_{DS}}{L}$$

① Constant Field Scaling:  
 ⇒ Parameter Before Scaling After scaling.

① Channel length

$L$

$$L' = L/s$$

② Channel width

$W$

$$W' = W/s$$

③ Gate oxide thickness

$t_{ox}$

$$t_{ox}' = t_{ox}/s$$

④ Junction depletion thickness

$x_j$

$$x_j' = x_j/s$$

⑤ Threshold voltage

$V_T$

$$V_T' = V_T/s$$

⑥ Power supply voltage

$V_{DD}$

$$V_{DD}' = V_{DD}/s$$

⑦ Substrate doping density

$N_A$

(or)

$N_D$

$$\frac{N_A'}{(or)} = s N_A$$

$$N_D' = s N_D$$

$$W \propto \sqrt{\left(\frac{1}{N_A} + \frac{1}{N_D}\right)}$$

② <u>Constant</u> Parameter	<u>Voltage</u>	<u>Scaling:</u>	
		Before Scaling	After Scaling.
① Channel length		$L$	$L' = L/s$
② Channel width		$W$	$W' = W/s$
③ Gate oxide thickness		$t_{ox}$	$t_{ox}' = t_{ox}/s$
④ Junction depletion thickness		$x_j$	$x_j' = x_j/s$
⑤ <u>Threshold Voltage</u>		<div style="border: 1px solid black; padding: 10px; display: inline-block;"> <math>V_T</math>                      <math>V_T</math>  <math>V_{DD}</math>                      <math>V_{DD}</math> </div>	
⑥ <u>Supply Voltage</u>			
⑦ Substrate doping density		$N_A$	$N_A' = s^2 N_A$
		(or) $N_D$	$N_D' = s^2 N_D$

### \* Level's of Integration:

- ① SSI: Such as 7404 has upto 10  
Gates per chip.  
ex: logic gates, flip-flop.
- ② MSI: Such as 7416 counter have upto  
1000 gates per chip.  
ex: Counters ICs,  
multiplexers, Adders.

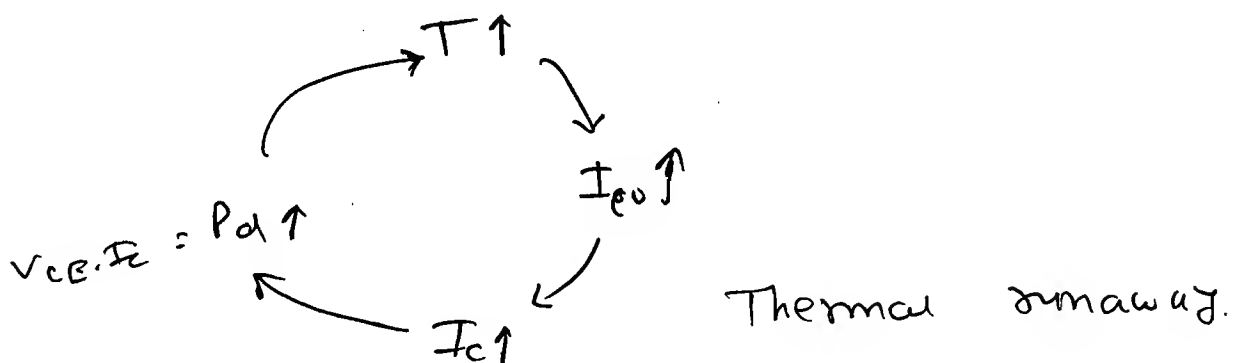
③ LST: Such as simple 8-bit  $\mu P$  have upto 10,000 gates per chip.  
Ex: 8-bit  $\mu P$ , Rom., RAM.

④ VLSI: more than 10,000 gates / chip.  
(or)  
1 million Transistor / chip.  
Ex: 16-bit  $\mu P$ , 32-bit  $\mu P$ .

1 - FET (Field Effect Transistor)

$\Rightarrow$  Advantages of FET.

- $\rightarrow$  Unipolar
- $\rightarrow$  Low Cost
- $\rightarrow$  Low noise
- $\rightarrow$  Low Power
- $\rightarrow$  Immune to radiation.
- $\rightarrow$  High i/p impedance (use in CRO, voltmeter).
- $\rightarrow$  Low offset voltage.
- $\rightarrow$  Low thermal sensitivity.



⇒ Thermal stability :

$$\frac{\partial P_d}{\partial T_j} < \frac{\partial P_o}{\partial T_j}$$

$$\Rightarrow V_{CE} < \frac{V_{CC}}{2}$$

→ BJT → CCCS

$$T_p \uparrow \rightarrow I_{B0} \uparrow \rightarrow I_E \uparrow$$

Positive temperature Coefficient.

→ FET → VCCS

$$T \uparrow \rightarrow I_D \downarrow$$

$$P_D = V_{DS} \cdot I_D$$

Negative temp. Coefficient.

\* Features of FET:

① Unipolar device because current is due to only majority carrier only.

② High input impedance.

③ Immune to Radiation.

④ Less noisy than BJT.

⑤ No offset voltage at zero drain

Current.

⑥ Thermally more stable than BJT.

⑦ Simple biasing.

→ It requires less no. of fabrication, diffusion steps therefore low cost.

→ Voltage Controlled devices that is VCCS.

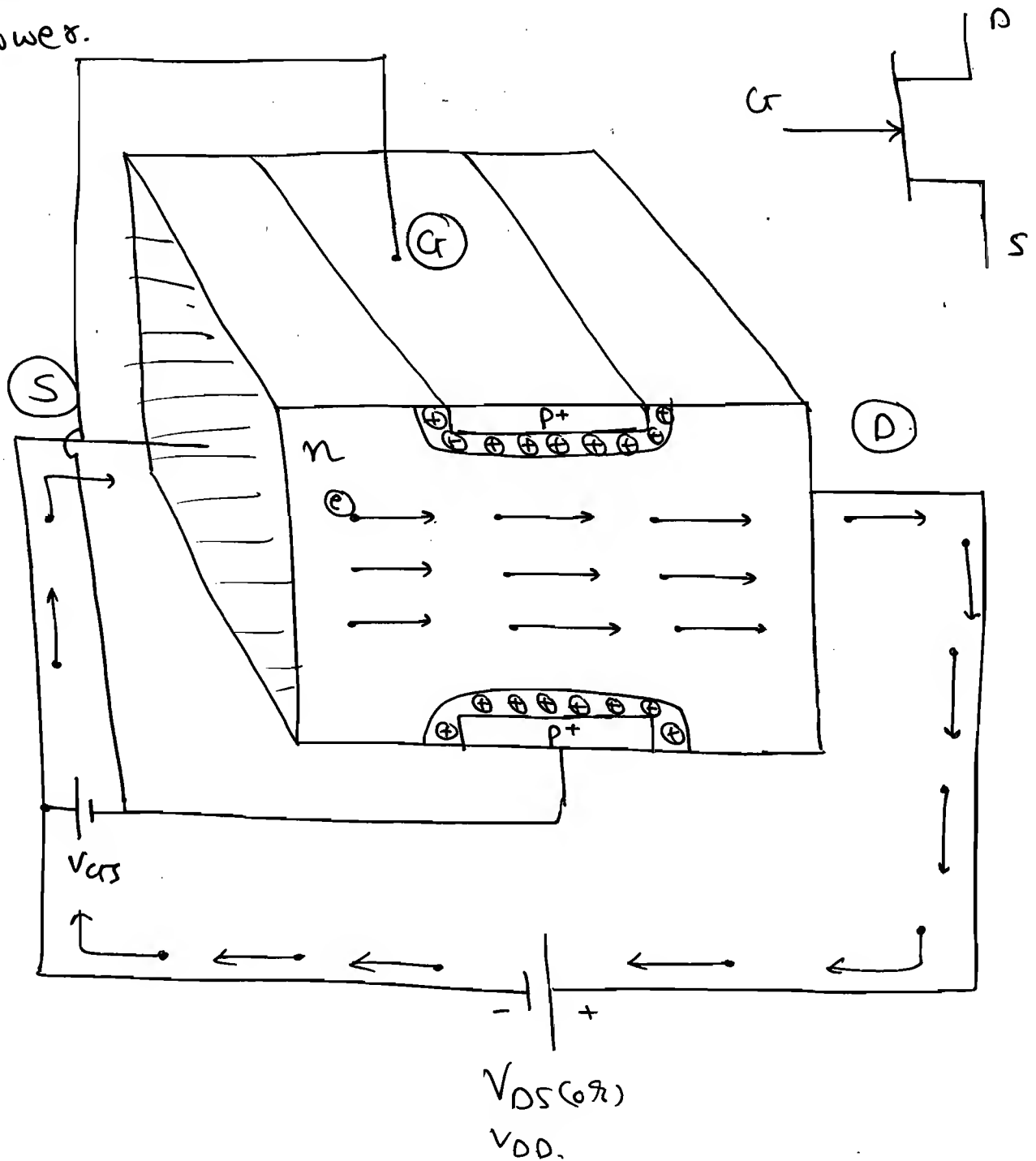
### \* Drawback:

→ Low gain Bandwidth Product.

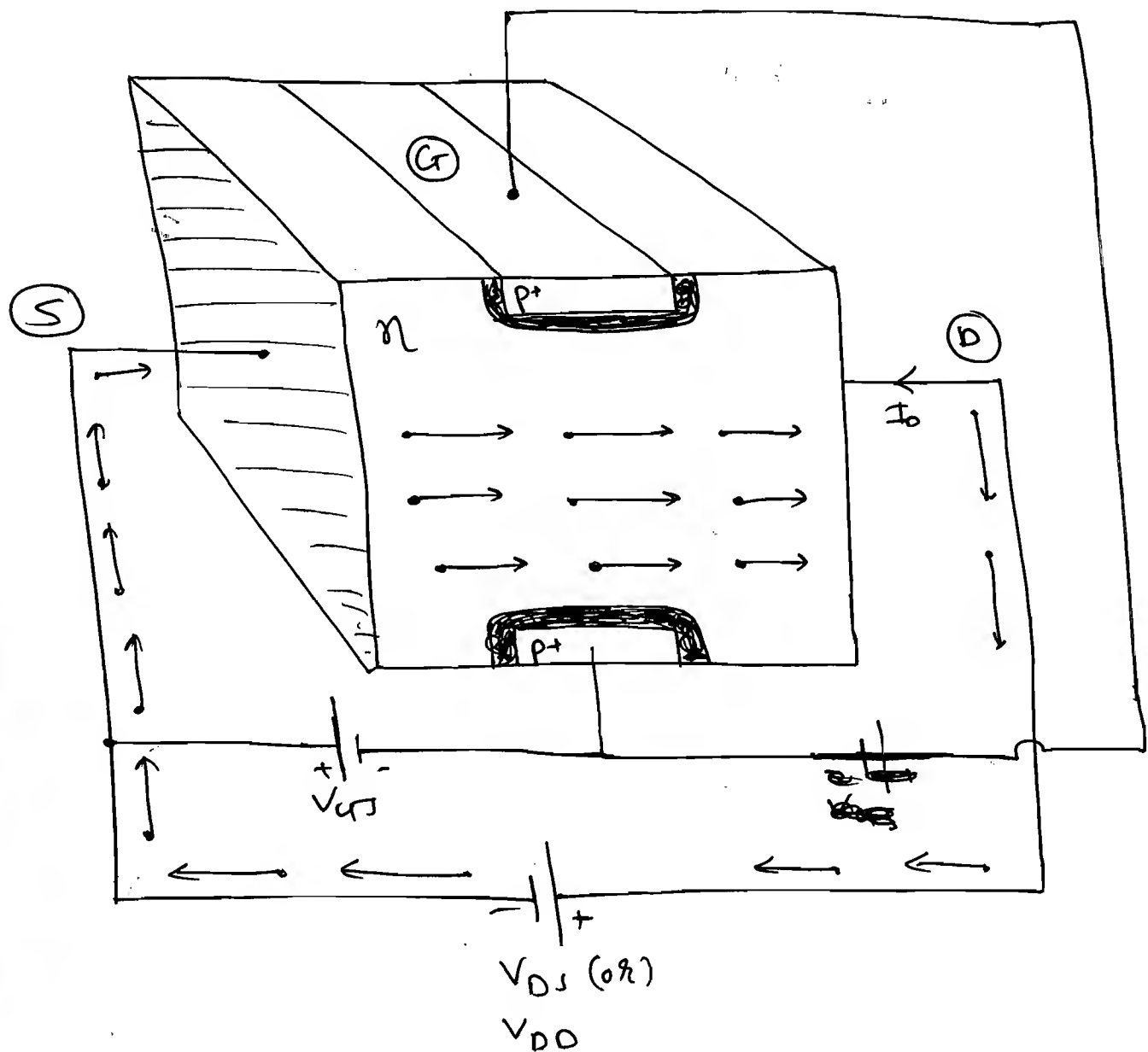
⇒ As transistor shrinks i.e. reduction in size it becomes faster & consumes less

Power.

⇒



\* n-channel JFET:



$$\begin{aligned} \Rightarrow I &= \frac{Q}{T} \\ &= \frac{Q_n}{T} \\ I &= \frac{Nq}{T} \end{aligned}$$

$$\Rightarrow I = \frac{-1.6 \times 10^{-19} N}{T}$$

① Source:

$\Rightarrow$  Source is the terminal through which majority carriers enter into the semiconductor bar.



8)

### \* Drain:

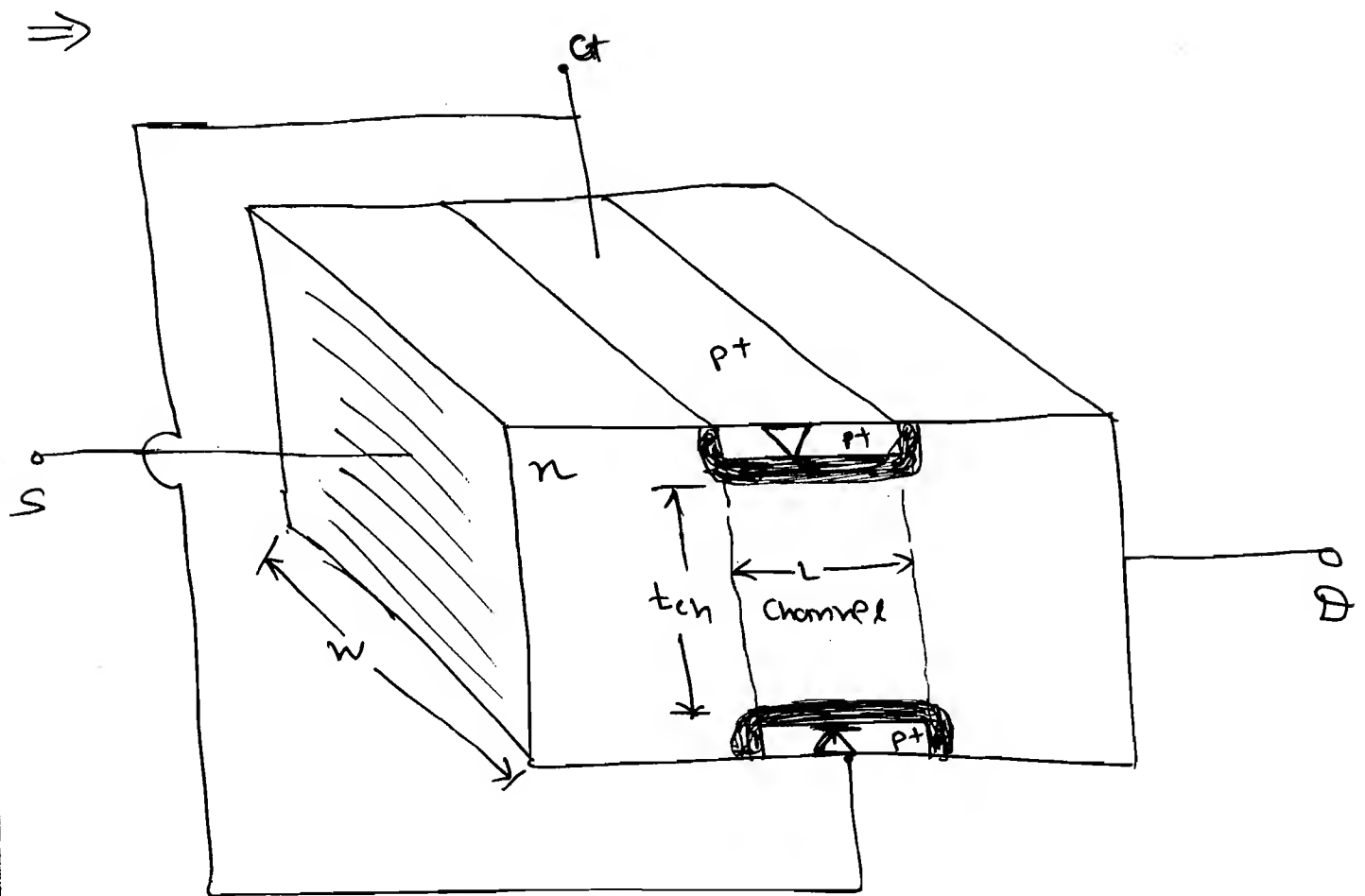
→ Drain is the terminal through which majority carriers are leaves from the semiconductor bar.

### \* Gate: ( $\alpha$ ):

⇒ Gate is the two heavily doped  $P^+$  regions diffused both the sides of the  $n$ -type semiconductor bar and it controls the flow of carriers ( $\alpha$ ) current bet<sup>n</sup> source and drain.

### \* Channel:

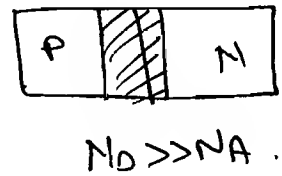
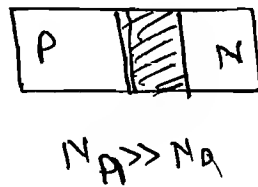
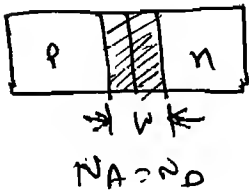
⇒ Channel is the region bet<sup>n</sup> two heavily doped  $P^+$  gate region through which carriers moves from source to drain.



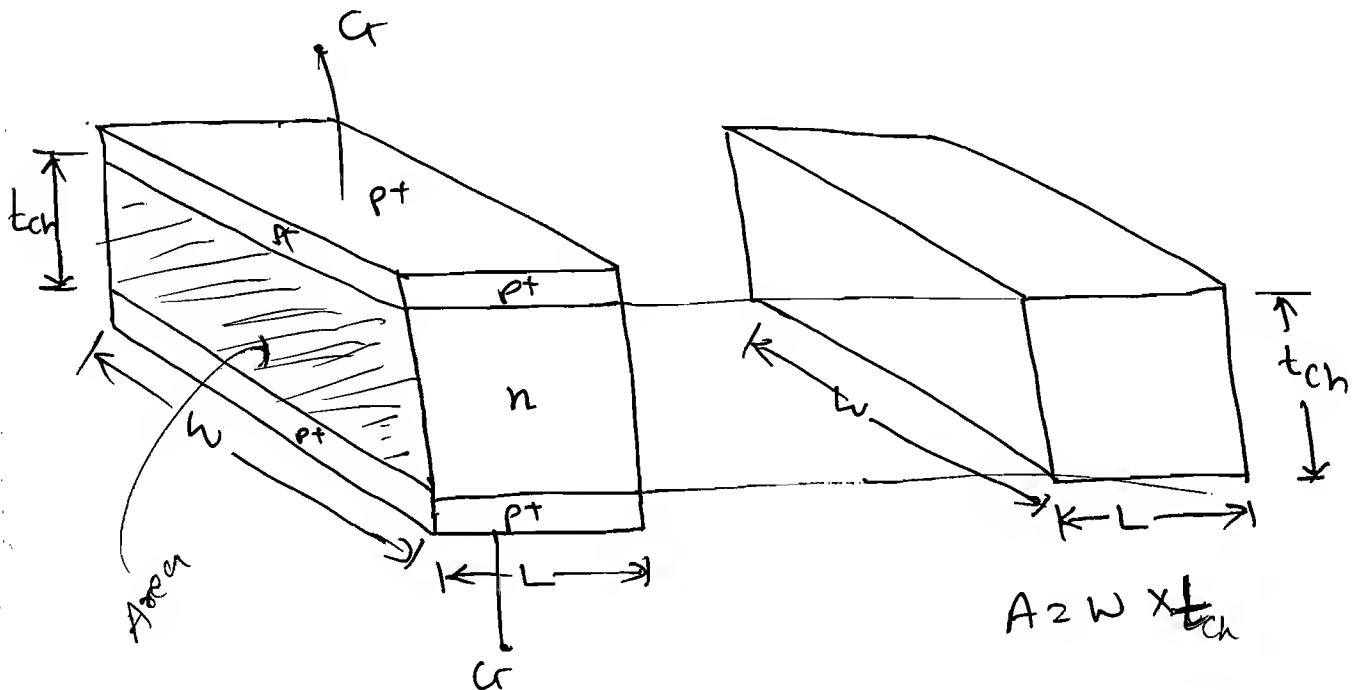
$$V_j = V_0$$

$$I_D \text{ (or) } I_{D1} = 0.$$

$$\omega \propto \sqrt{\frac{1}{N_A} + \frac{1}{N_D}}$$



⇒ Channel Portion:



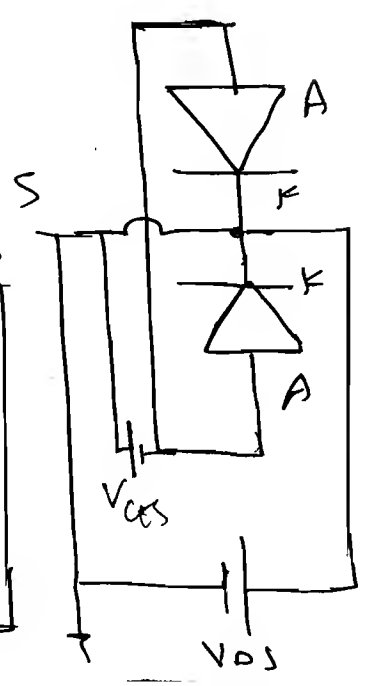
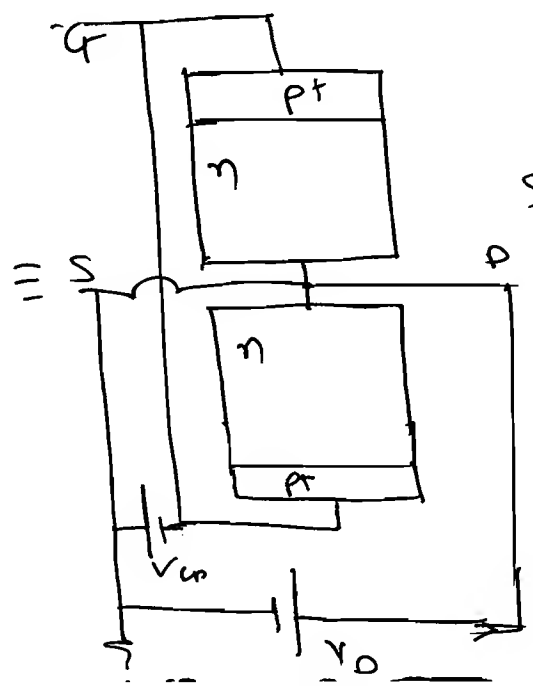
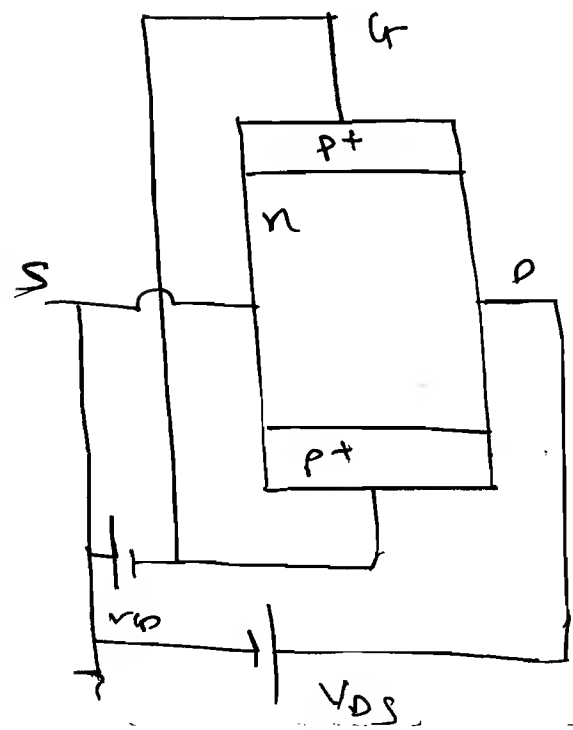
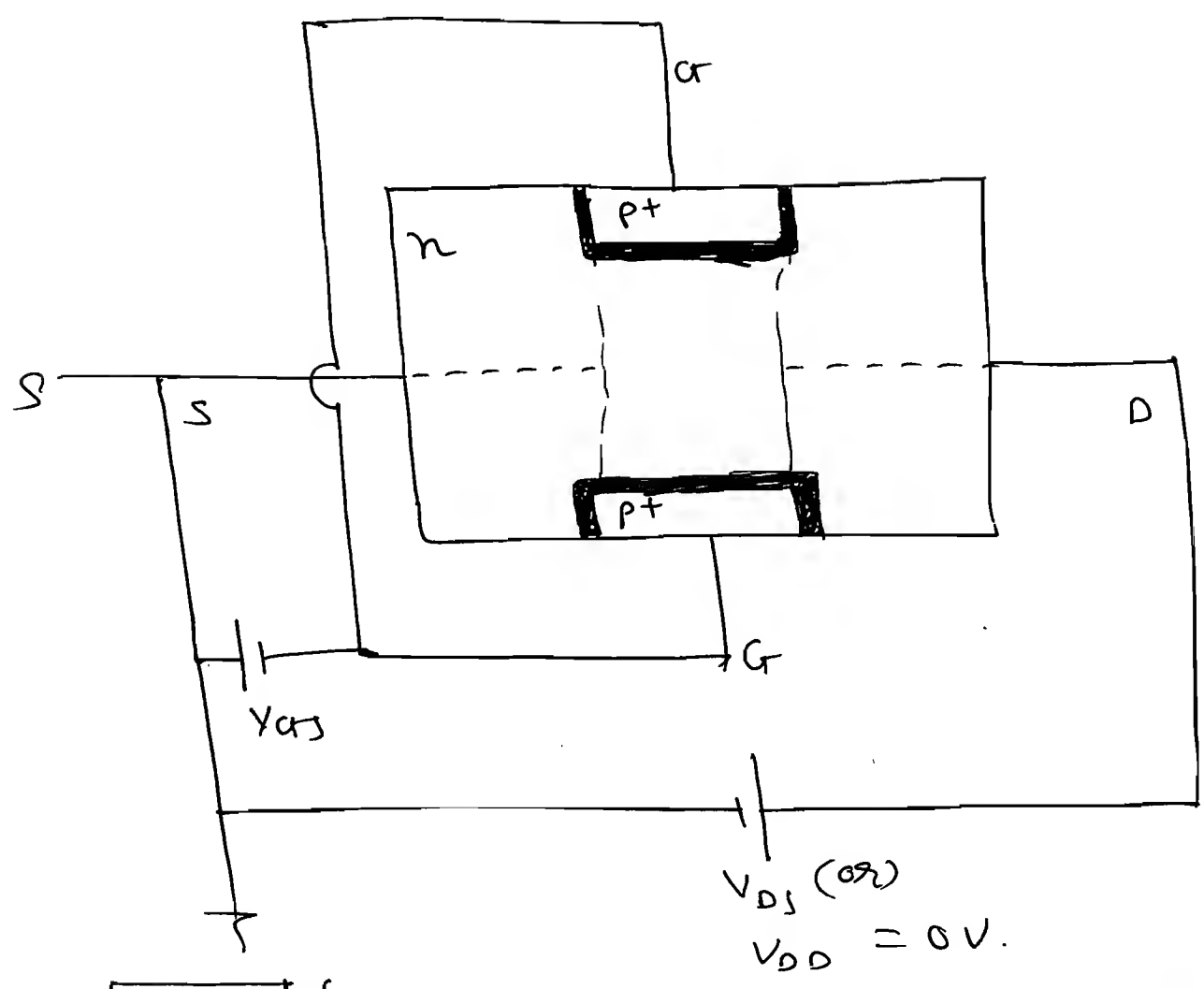
$$\rightarrow R = \frac{\rho L}{A}$$

$$\rho_n = \frac{1}{n e \mu_n} \approx \frac{1}{N_D \mu_n}$$

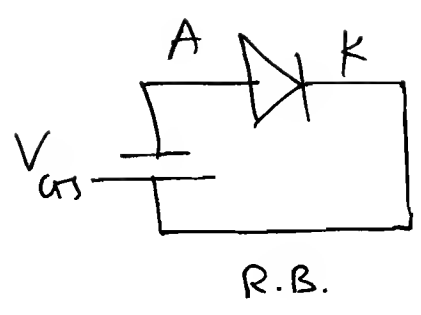
$$R_{ch} = \frac{\rho L}{A}$$

Let,  $R_{ch} = 500 \Omega$ .

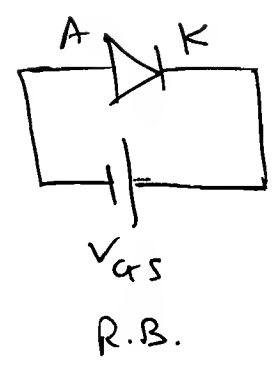
$\Rightarrow$



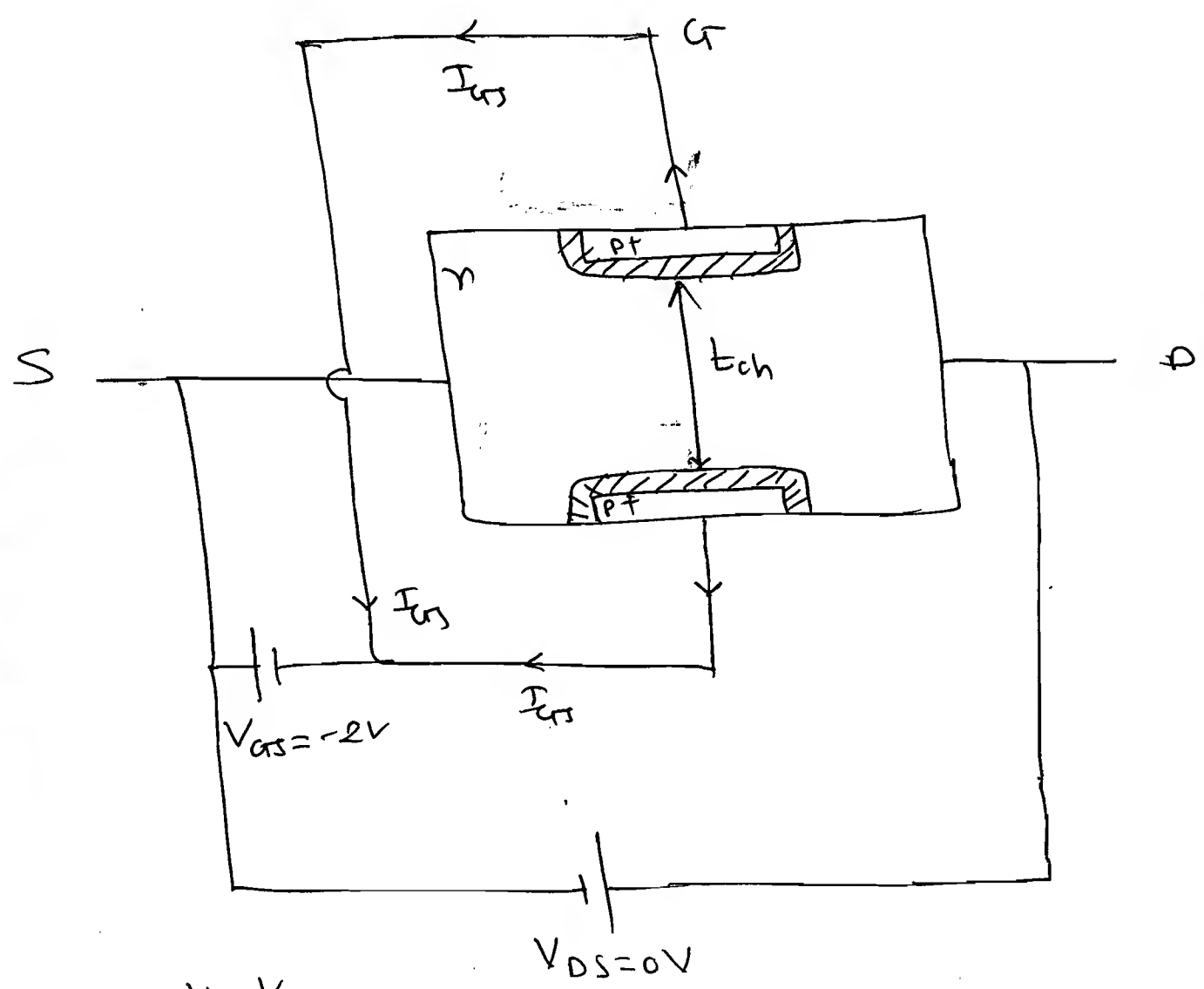
⇒



≡



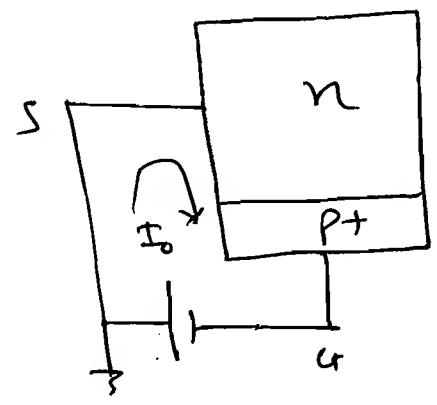
⇒ When  $V_{GS} = -2V$  &  $V_{DS} = 0V$



$$V_j = V_0 + V_{GS}$$

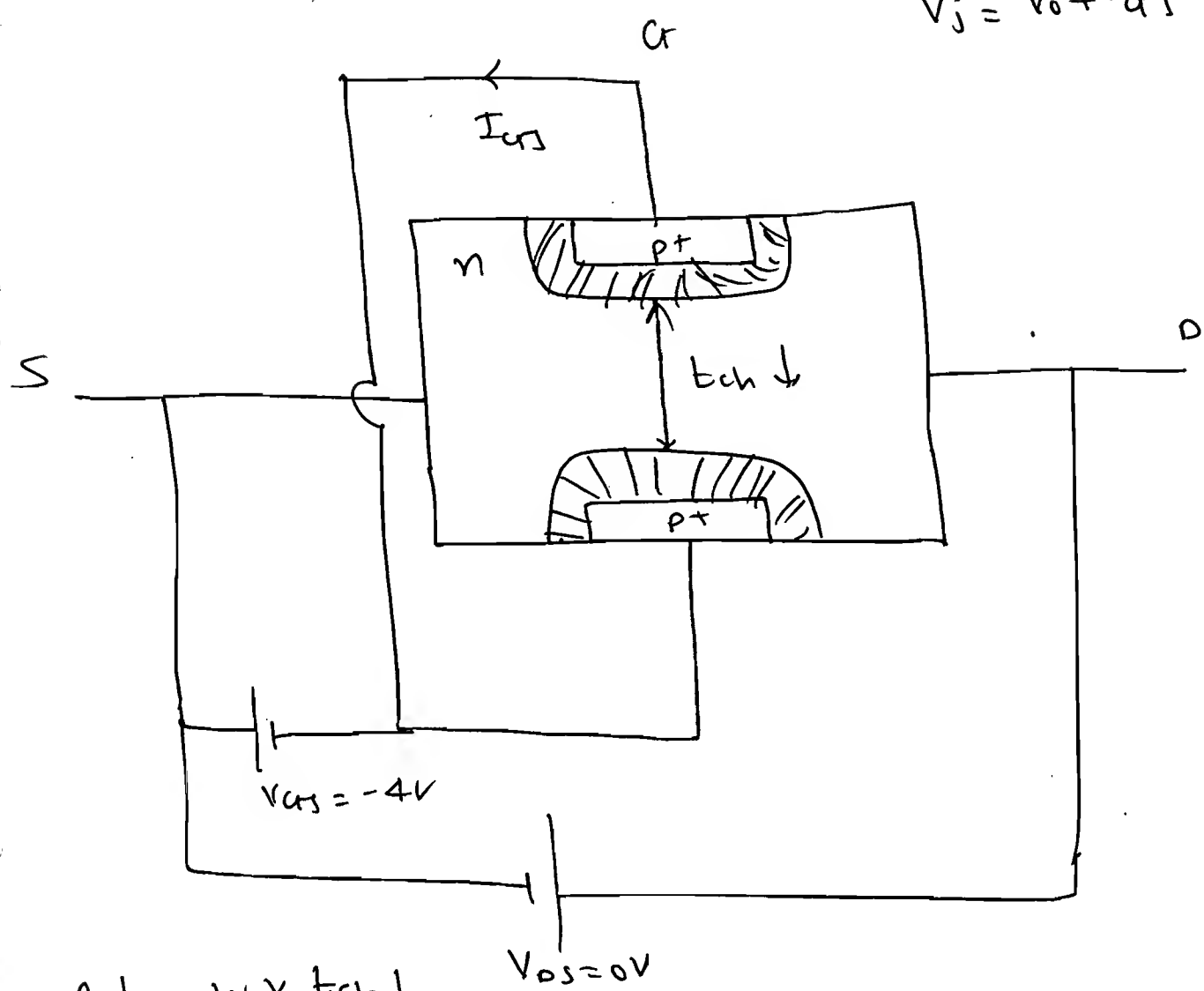
$$A \downarrow = W \times t_{ch} \downarrow$$

$$R \uparrow = \frac{\rho L}{A \downarrow}$$



$\Rightarrow$  When  $V_{GS} = -4V$ .

$$V_j = V_0 + V_{GS}$$



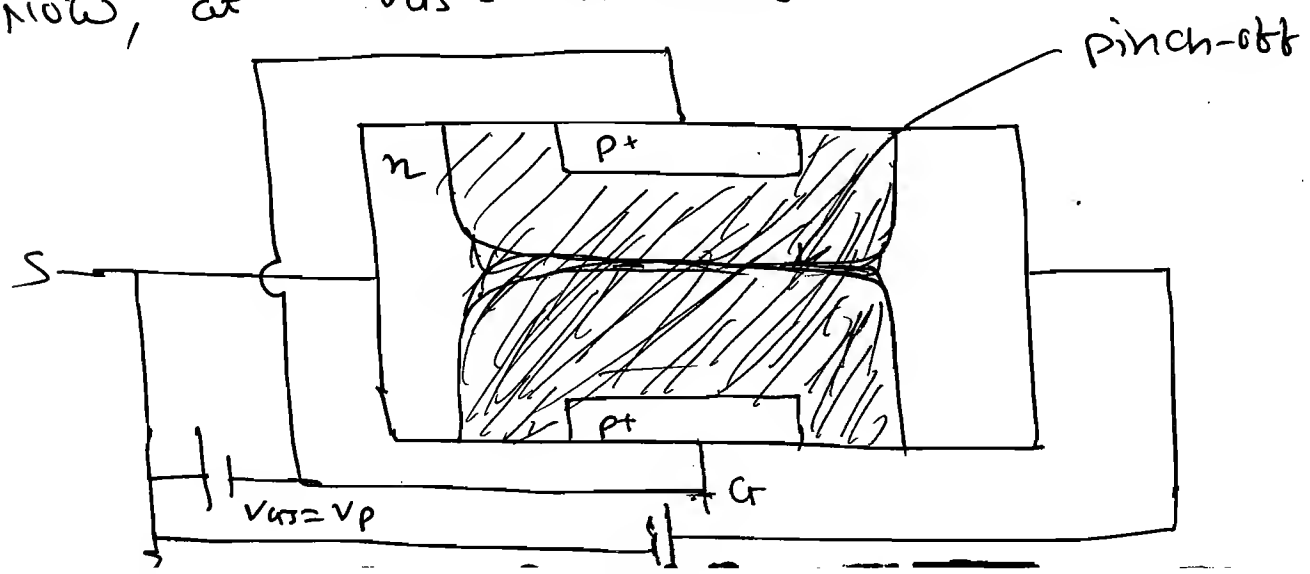
$$A \downarrow = w \times t_{ch} \downarrow$$

$$V_{DS} = 0V$$

$$\uparrow R \downarrow \frac{SL}{A \downarrow}$$

$\Rightarrow$  So, this JFET can be used as Voltage Regulator Variable Resistor.

Now, at  $V_{GS} = V_{GS(cutoff)} = V_p$ .



$$V_j = V_0 + V_{crs} \text{ (cut-off)}.$$

$$\Rightarrow t_{ch} = 0 \Rightarrow A = w \times t_{ch} \approx 0 \text{ m}^2.$$

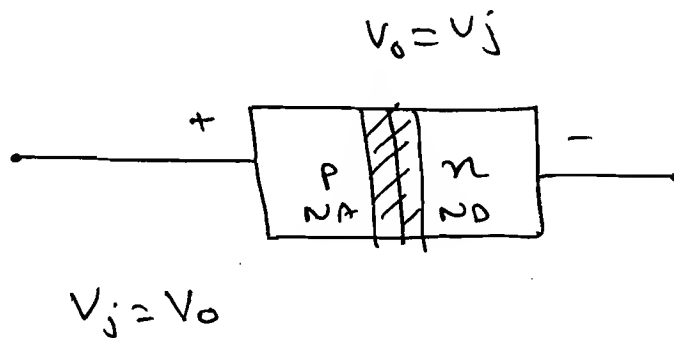
$$\Rightarrow R = \frac{\rho L}{A} = \infty \Omega.$$

$$\Rightarrow R_{ch} = \infty \Omega \text{ So. open circuit.}$$

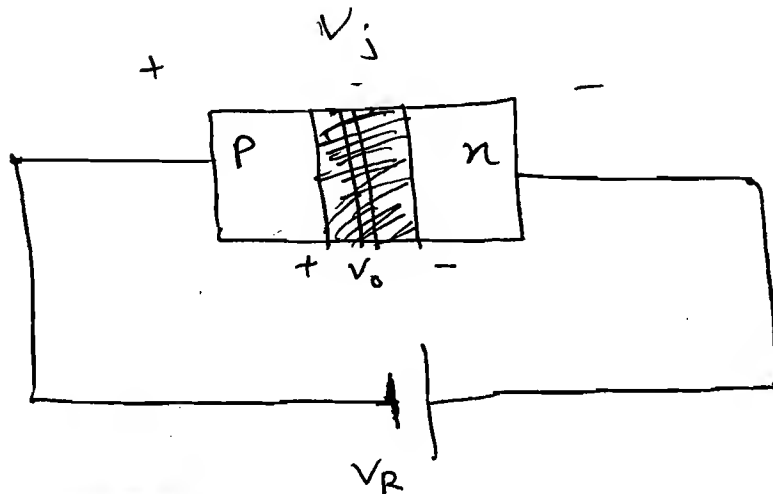
i.e. JFET is OFF or in cut-off.

$\Rightarrow$  At particular value of  $V_{crs}$ , thickness of the channel is almost zero and no carrier is flow from source to drain end hence no current flow and JFET comes into cut-off. This condition is called pinch-off and it ranges from  $-9V$  to  $-25V$ .

$\Rightarrow$  O.C.

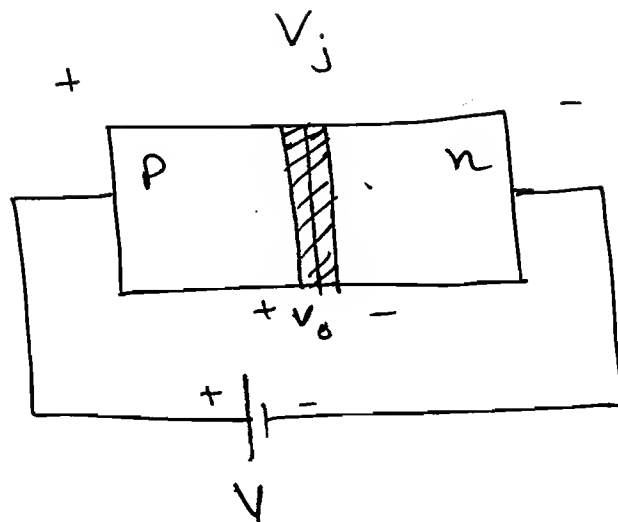


$\Rightarrow$  R.B.



$$V_j = V_0 + V_R.$$

$\Rightarrow$  F.B.



$\therefore$  By KVL,  $V - V_j - V_0 = 0.$

$$\therefore V_j = V - V_0.$$

$$V_j = V_0 - V_F.$$

$$\Rightarrow V_{GS}(\text{cut-off}) = V_{GS}(\text{off}) = V_P.$$

$\Rightarrow$  Condition for pinch-off:

$$\therefore V_{DS} = V_{GS} - V_P.$$

$$\therefore 0 = V_{GS} - V_P \Rightarrow V_{GS} = V_P = -10V.$$

$$\Rightarrow I_{RSS} \rightarrow nA$$

$I_{RSS}$ : Reverse Saturation Current

: Depend on temp.

: Inc by  $7\% / ^\circ C$ .

: Double  $/ 10^\circ C$ .

$I_{RSS}$  at  $T_1$  (given)

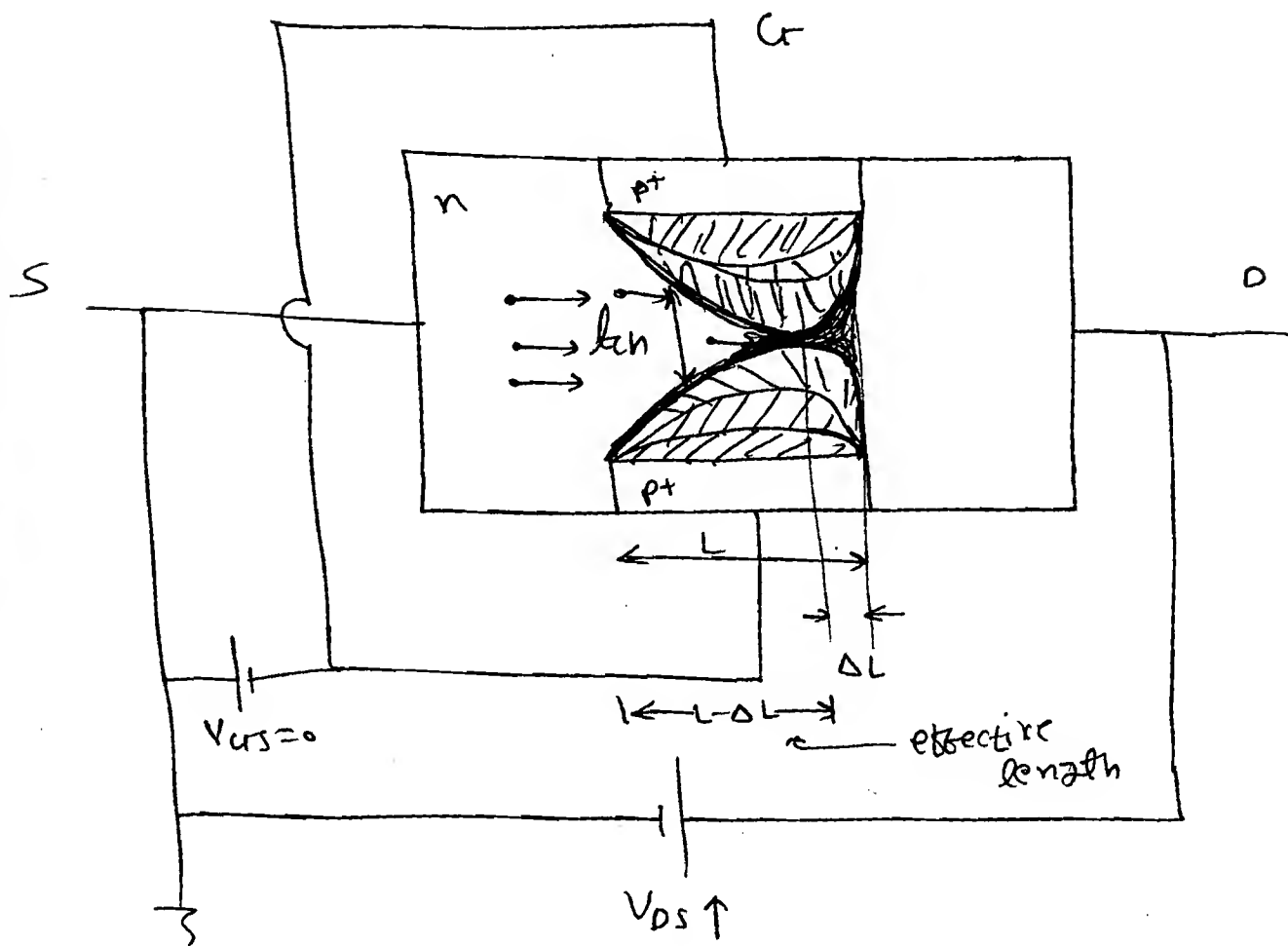
$I_{RSS}$  at  $T_2 = ?$

$$\Rightarrow \frac{I_{DSS}(T_2)}{I_{DSS}(T_1)} = 2^{\frac{T_2 - T_1}{10}}$$

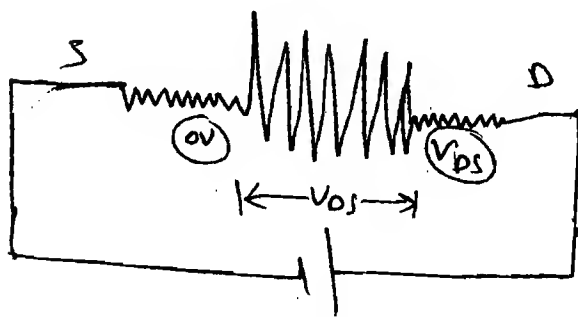
$$I_{DSS}(T_2) = 2^{\frac{T_2 - T_1}{10}} \cdot I_{DSS}(T_1)$$

$$I_{O2} = 2^{\frac{T_2 - T_1}{10}} \cdot I_{O1}(T_1)$$

Case-ii Now,  $V_{GS} = 0$ ,

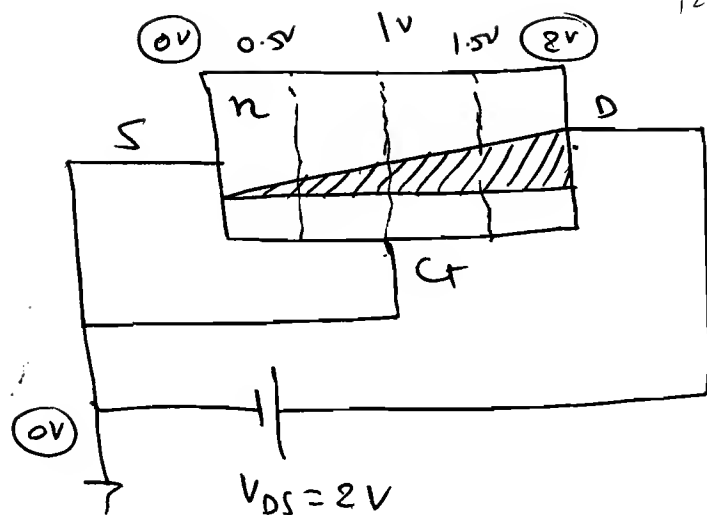
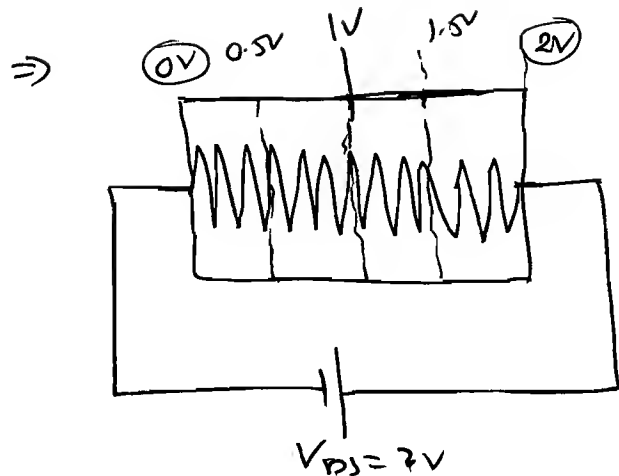


$\Rightarrow$  Resistance across the channel:



When we move from source to drain channel resistor is increased.



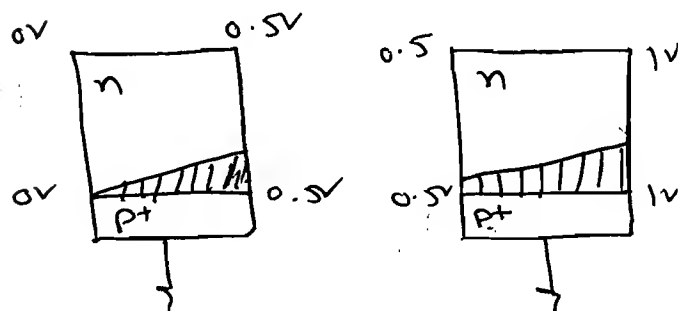


⇒  $E \uparrow = \frac{V_{DS}}{L} \uparrow$

$V \propto E$

⇒  $V_{DS} \propto E$

⇒  $I_{DS} \propto V_{DS}$



\* Condition for pinch-off:

⇒  $V_{DS} = V_{GS} - V_P$

∴  $V_{DS} = 0 - V_P$

$V_{DS} = -V_P = -(-10) = 10V$

⇒  $E = \frac{\Delta V_{DS}}{\Delta L}$

⇒ At  $\Delta L$  portion  $E$  is constant.

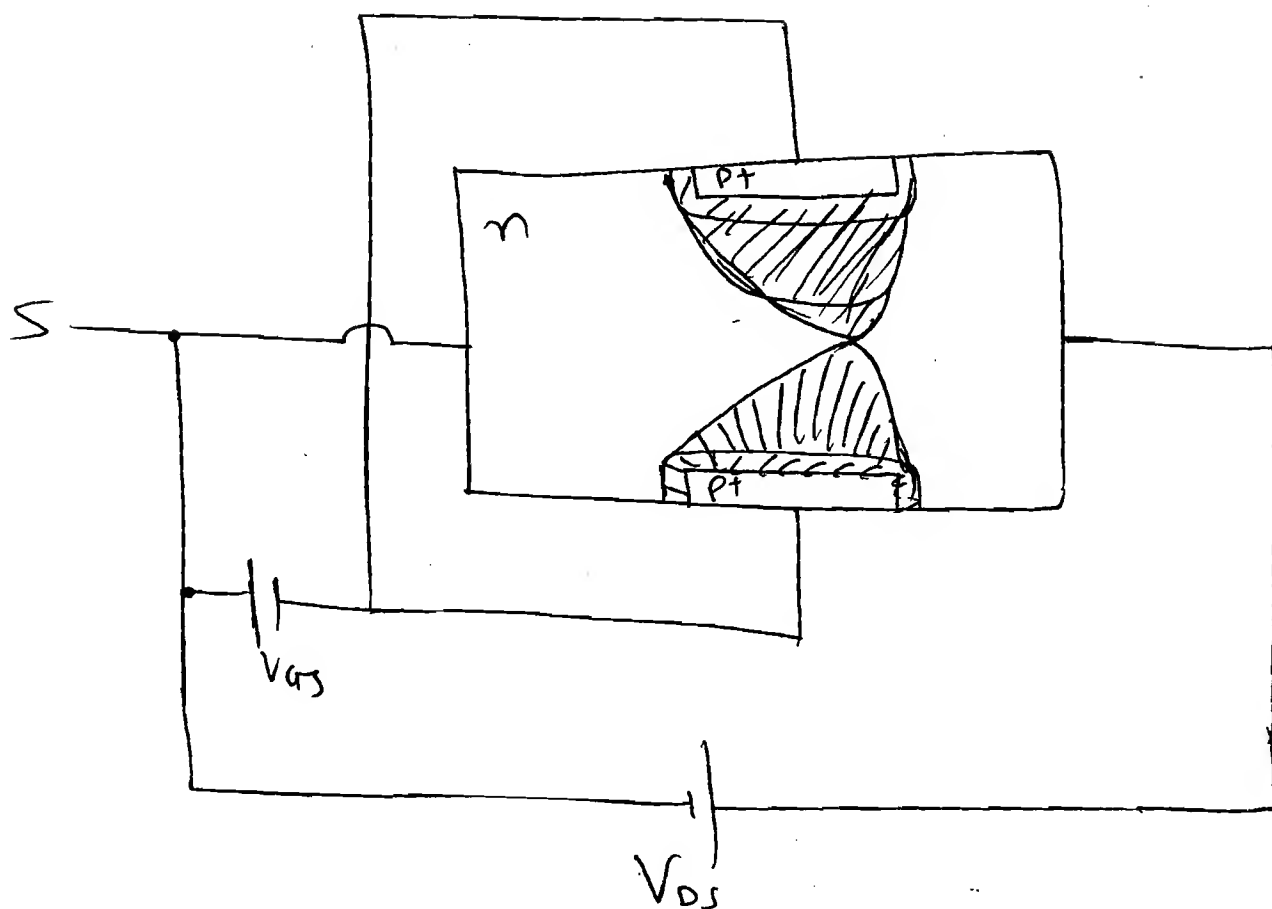
⇒  $I_D$  (or)  $I_{DS} = I_S$

⇒  $V_j = V_0 + V_{GS} + V_{DS}$

Note: In BJT we decide region of operation based on biasing of BE and CB junction. In JFET we will decide the region of operation based on the  $I_D$  current. In Sat' region

$I_D$  remains constant.

$\Rightarrow$



$$V_j = V_0 + V_{GS} + V_{DS}$$

$$\Rightarrow V_{DS} = V_{GS} - V_P$$

$$V_{GS} - V_P = -2V - (-10V) = 8V$$

if  $V_{DS} = 8V$

$$\Rightarrow V_{DS} = V_{GS} - V_P$$

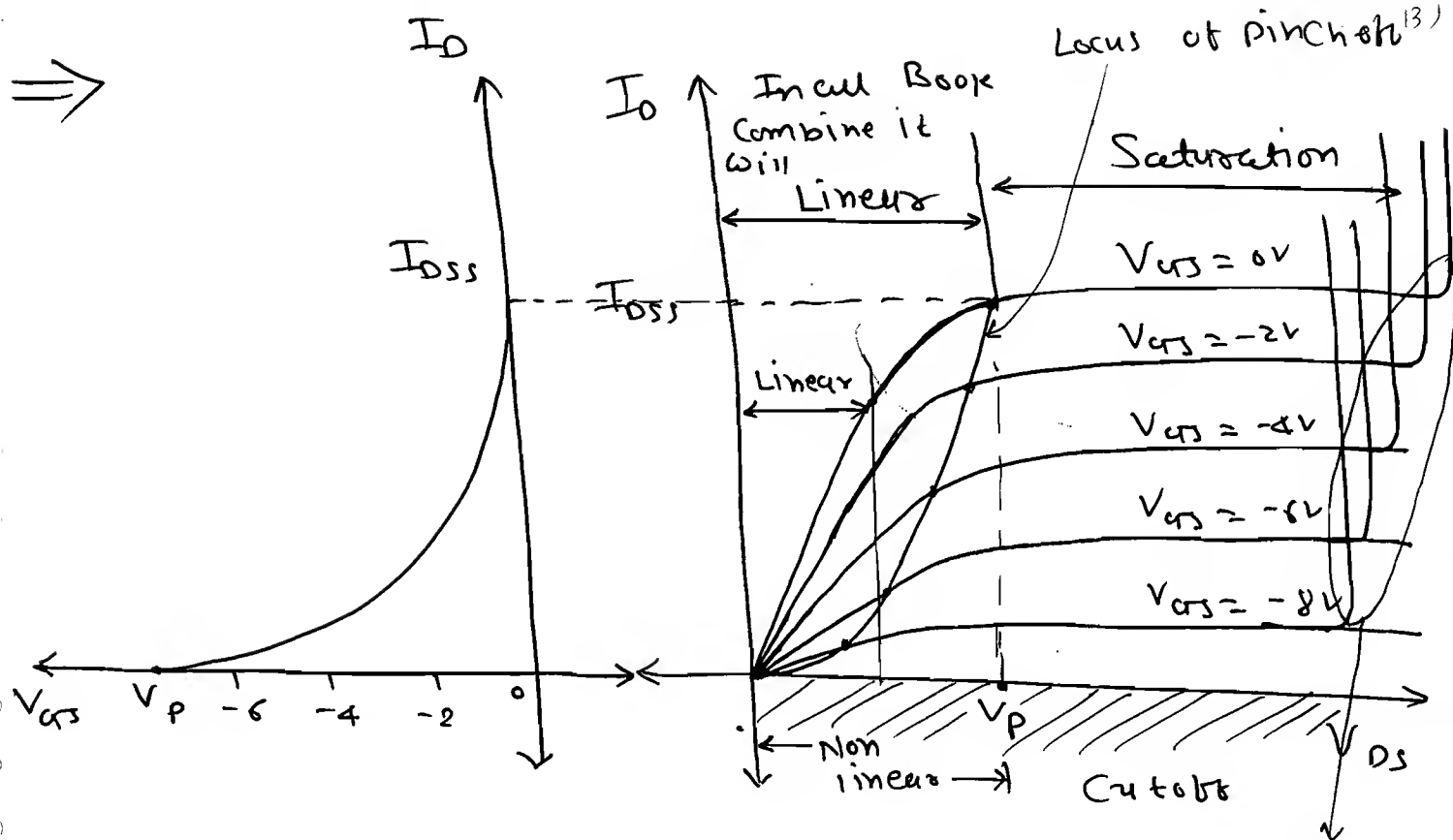
if  $V_{DS} = 7V$

$$\Rightarrow V_{DS} < V_{GS} - V_P \Rightarrow \text{operate in linear region.}$$

if  $V_{DS} = 10V$

$$\Rightarrow V_{DS} > V_{GS} - V_P \Rightarrow \text{operate in sat. region.}$$

$$\left. \begin{array}{l} V_P = -10V \\ V_{GS} = -10 \end{array} \right\} V_{GS} = V_P \left. \begin{array}{l} V_P = -10V \\ V_{GS} = -12 \end{array} \right\} V_{GS} < V_P \left. \begin{array}{l} V_{GS} = V_P \\ V_{GS} < V_P \end{array} \right\} V_{GS} \leq V_P \Rightarrow \text{cut-off.}$$



(Transfer characteristics)

(Drain characteristics)

⇒ To find the region of operation  $V_{GS}$ ,  $V_{DS}$  &  $V_P$  should be known.

→ if  $V_{GS} \leq V_P \rightarrow$  Cut-off

→  $V_P < V_{GS} < 0$ .

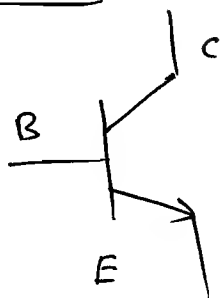
Calculate  $V_{GS} - V_P$ :

- |  |
|--|
| • if $V_{DS} < V_{GS} - V_P =$ linear      |
| • if $V_{DS} > V_{GS} - V_P =$ Saturation. |

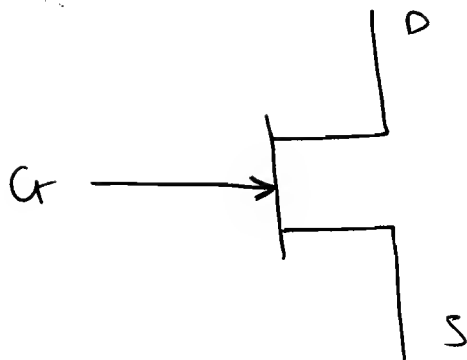
⇒  $BV_{DS}$  = Drain to Source Breakdown voltage.

\* Symbol:

⇒ BJT:



Same Concept as in RJT



Direction of arrow decided Based on emitter current.

For npn it leaves and pnp it enters to the Base.

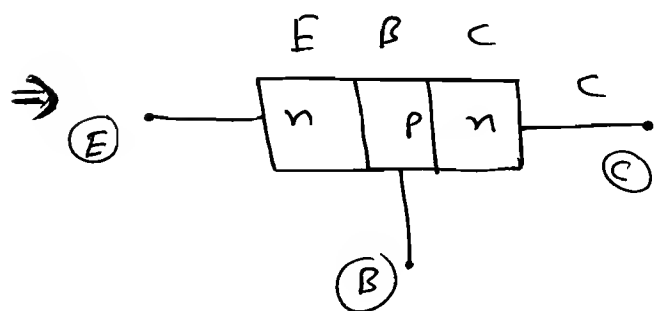
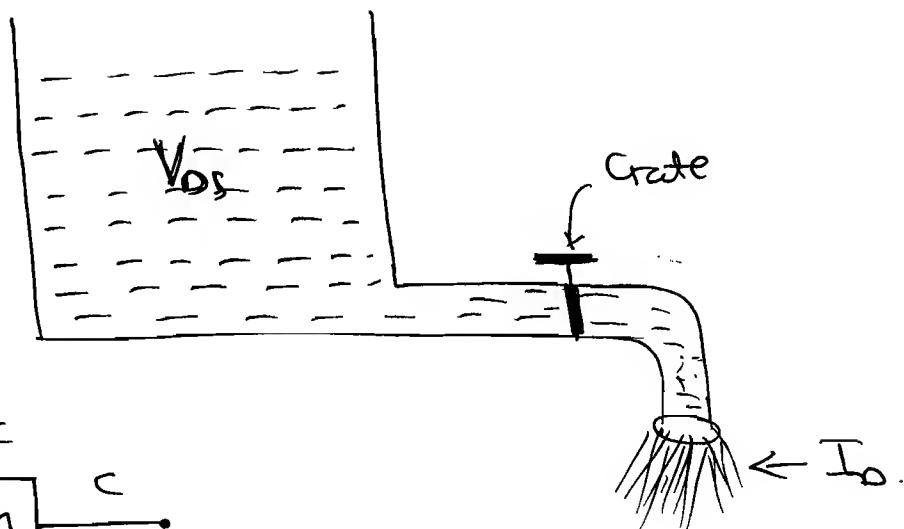
→ At  $V_{GS} = 0 \Rightarrow I_D = I_{DSS}$

→  $I_D \leq I_{DSS}$

→ At  $V_{GS} = 0$

$I_S = I_D = I_{DSS}$

⇒



⇒ BJT is not a ~~uni~~ bilateral device. It is a ~~b~~ unilateral device. Because if we change of <sup>polarity</sup> supply the current will not same. Because in BJT Carrier Concentration is not same in C & E. In BJT Collector is collector

14)  
Emitter is omitted.

$\Rightarrow$  Where as in JFET Drain and Source can be interchanged.

$\Rightarrow$  A Kya

\* Important points to be remember in  
n-channel JFET.

$\Rightarrow$  n-Channel JFET operates with -ve gate to source voltage. i.e. -ve  $V_{GS}$  values.

$\Rightarrow$  Gate to Source Voltage and pinch-off Voltages are -ve for n-channel JFET.

$\Rightarrow$  n-JFET operates in depletion mode for -ve  $V_{GS}$  values.

$\Rightarrow$  JFET operates always in depletion mode.

$\Rightarrow$  JFET operates with reversed biased gate junction.

$\Rightarrow$   $V_{GS(\text{cut-off})}$  Voltage is the value of the  $V_{GS}$  at which both the gate depletion regions comes close and the thickness of the channel becomes zero and also drain current  $I_D = 0$ . ( $V_{DS} = 0$ ).

$\Rightarrow$  pinch-off Voltage is the minimum value of  $V_{GS}$  at which drain ~~and~~ current

becomes constant. ( $V_{as}=0$ ).  
⇒ The relation bet<sup>n</sup>  $V_{as}$  (cut-off) Voltage  
and  $V_p$  is  $V_{as}(\text{cut-off}) = V_{as}(\text{ofs}) = V_p$ .

⇒ In n-channel JFET as  $V_{as}$  decreases  
(i.e. increasing in -ve direction) pinch-off  
Voltages happens for lower values of  
 $V_{DS}$ .

⇒ Condition for pinch-off (or) Saturation  
is  $V_{DS} = V_{as} - V_p$   
(+ve) (-ve) (-ve)

⇒ In n-JFET as  $V_{as}$  increases avalanche  
break-down happens due to avalanche effect  
for lower values of  $V_{DS}$ .

⇒ JFET operates in linear, saturation  
and cut-off region.

⇒ Linear region is the region which is left  
side to the pinch-off locus.

⇒ Sat. region is the region Right side to  
the pinch-off locus.

⇒ Cut-off region is the region below  $V_{as} = V_p$ .

$\Rightarrow$  JFET can be used as Amplifier in <sup>(15)</sup> a Sat. region and it can be used as a Switch in a linear and cut-off regions.

$\Rightarrow$  JFET can be used as Voltage Variable Resistor in linear region and it can be operate as a Current Source in Saturation region.

$\Rightarrow$  Linear region is also called as 'ohmic region' (or) triode region.

$\Rightarrow$  Transfer Char. of a JFET gives pinch-off Voltage ( $V_p$ ),  $I_{DSS}$  and Trans conductance ( $g_m$ ).

$\Rightarrow$  For  $V_{GS} \leq V_p$  n-channel JFET operates in cut-off region and its drain current  $I_D = 0A$ .

$\Rightarrow$  For  $V_p < V_{GS} < 0$  &  $V_{DS} < V_{GS} - V_p$  it operates in linear region and its drain current

$$\therefore I_D = \frac{2 I_{DSS}}{V_p^2} \left[ \underset{\substack{\uparrow \\ -ve}}{(V_{GS} - V_p)} \underset{\substack{\uparrow \\ -ve}}{V_{DS}} - \frac{1}{2} \underset{\substack{\uparrow \\ +ve}}{V_{DS}^2} \right]$$

$\Rightarrow$  For  $V_p < V_{GS} < 0$  and  $V_{DS} \geq V_{GS} - V_p$  it operates in sat region, and its drain

current

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_p} \right]^2$$

-ve  
-ve

Note:

⇒ JFET is a Symmetrical device  
therefore Source and Drain terminal  
can be interchanged.

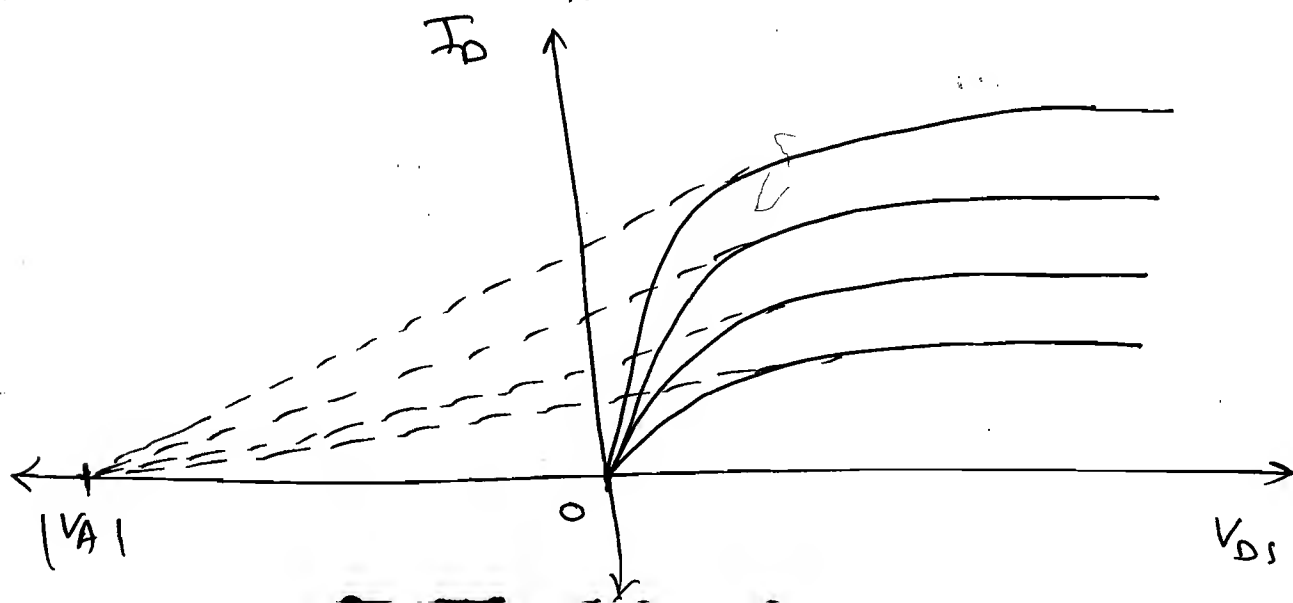
\* Channel Length Modulation:

⇒ In Saturation region as drain to  
Source voltage increases the effective  
length of the channel is decreases i.e.  
as  $V_{DS}$  varies, the length of the  
Channel is also varies. i.e. called Channel  
length Modulation. Due to Channel length  
Modulation Drain Current increases as

$$I_D = I_{DSS} \left[ 1 - \frac{V_{DS}}{V_P} \right]^2 (1 + \lambda V_{DS}).$$

Where,  $\lambda$  is Channel length modulation  
parameter.

$$\lambda = \frac{1}{V_A}, \quad V_A = \text{Early Voltage.}$$





\* Drain Resistance (or) o/p resistance: (1)

⇒ It is the Resistance offered by the JFET in the Sat. region.

⇒ It is the reciprocal of the slope of Drain characteristics in the ~~the~~ saturation region.

$$\Rightarrow r_d \text{ (or) } r_o = \frac{1}{\left. \frac{\Delta I_D}{\Delta V_{DS}} \right|_{V_{GS}}} = \left. \frac{dV_{DS}}{dI_D} \right|_{V_{GS}}$$

⇒ Drain Resistance (or) o/p Resistance are also called Ac resistance (or) Small signal resistance.

$$\Rightarrow r_d \text{ (or) } r_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D} \quad (\because \frac{1}{\lambda} = V_A)$$

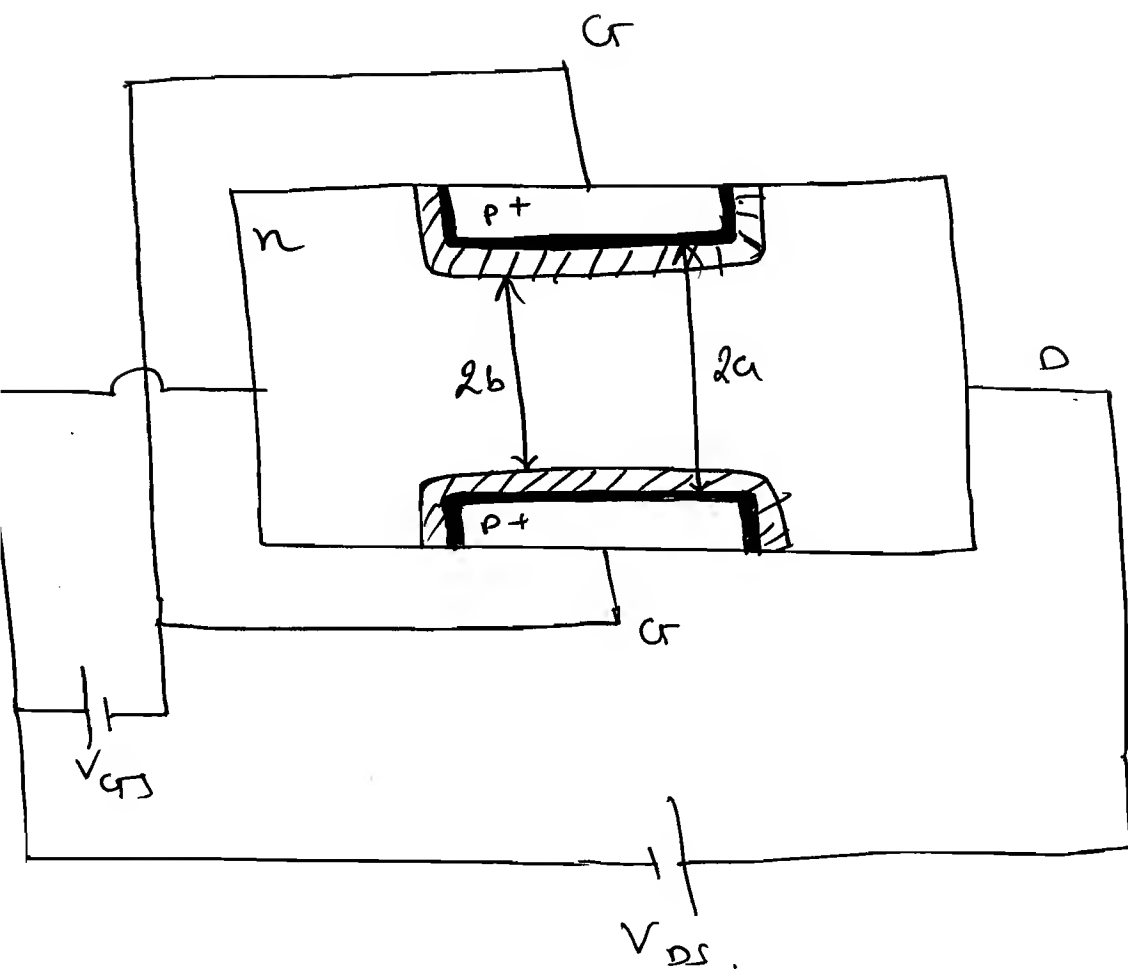
→ It ranges from  $50 \text{ k}\Omega$  to  $100 \text{ k}\Omega$ .

\* Trans Conductance ( $g_m$ ):

⇒ Trans Conductance is also called as mutual Conductance (or) figure of merit.

⇒ It gives how effectively JFET converts Voltage changes at the input to the corresponding current changes at the o/p in the saturation region.

$$g_m = \left. \frac{\Delta I_D}{\Delta V_{GS}} \right|_{V_{DS}} = \left. \frac{dI_D}{dV_{GS}} \right|_{V_{DS}}$$



$a$  = half-channel thickness (or) width at  $V_{gs} = 0V$ .  
 $b$  = half-channel thickness (or) width at a given  $V_{gs}$ .

Pinch-off Voltage of n-JFET:

$$V_p = \frac{e N_D}{2 \epsilon} \cdot a^2 \Rightarrow V_p = -ve$$

$$e = -1.6 \times 10^{-19} \text{ C.}$$

$\epsilon$  = Permittivity of Si

$$\epsilon = \epsilon_0 \epsilon_r$$

$$\epsilon_r = 11.7 \approx 12$$

$$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m.}$$

$$\epsilon_0 = 8.85 \times 10^{-14} \text{ F/cm.}$$

$a$  = half-channel thickness at  $V_{gs} = 0$ .

⇒ Pinch-off Voltage of a P-JFET:

18)

$$\rightarrow V_p = \frac{e N_A}{2 \epsilon} \cdot a^2$$

$e = 1.6 \times 10^{-19} \text{ C}$  = charge of hole

$N_A$  = acceptor concentration.

$$V_p = +ve$$

\* Relation B/w  $V_{GS}$  &  $V_p$ :

$$\Rightarrow V_{GS} = [1 - b/a]^2 \cdot V_p$$

$$\Rightarrow b = a \left[ 1 - \sqrt{\frac{V_{GS}}{V_p}} \right]$$

Ex-1 An n-channel JFET has channel thickness of  $10 \mu\text{m}$  at  $V_{GS} = 0\text{V}$ . Calculate its channel thickness at  $V_{GS} = -5\text{V}$ . Assume  $V_p = -10\text{V}$ .

Soln: Here,  $2a = 10 \mu\text{m}$  &  $2b = ?$   
 $V_p = -10\text{V}$

$$\therefore 2b = a \left[ 1 - \sqrt{\frac{V_{GS}}{V_p}} \right]$$

$$\therefore 2b = 2a \left[ 1 - \sqrt{\frac{V_{GS}}{V_p}} \right]$$

$$\therefore 2b = 10 \mu\text{m} \left[ 1 - \sqrt{\frac{-5}{-10}} \right]$$

$$\Rightarrow 2b = 10 \mu\text{m} \left[ 1 - \frac{1}{\sqrt{2}} \right]$$

$$2b = 2.93 \mu\text{m}$$

= thickness of channel at  $V_{GS} = -5\text{V}$ .

\* Drain ON Resistance (or) ON Resistance

$$\Rightarrow r_{don} \text{ (or) } r_{ds(on)} \text{ (or) } r_{(on)}$$

$\Rightarrow$  It is the resistance offered by the JFET in linear region. for small value of  $V_{DS}$ .

$\Rightarrow$  It is the reciprocal of the slope of the drain characteristics in the linear region. for small value of  $V_{DS}$ .

$$\Rightarrow R_{ON} = \frac{1}{\frac{\Delta I_D}{\Delta V_{DS}}} \bigg|_{V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \bigg|_{V_{GS}}$$

$$= \frac{dV_{DS}}{dI_D} \bigg|_{V_{GS}}$$

$$r_{d(on)} = \frac{L}{2\mu n N_A \ln 2 \left[ 1 - \sqrt{\frac{V_{GS}}{V_P}} \right]}$$

$r_{d(on)}$  = Drain ON resistance at a given  $V_{GS}$ .

$$\Rightarrow \text{At } V_{GS} = 0V$$

$$\Rightarrow r_{d0(on)} = \frac{L}{2\mu n N_A \ln 2} \bigg|_{V_{GS}=0}$$

$$\therefore r_{d(on)} = \frac{r_{d0(on)}}{\left( 1 - \sqrt{\frac{V_{GS}}{V_P}} \right)}$$

$\Rightarrow r_{d(on)} > r_{d0(on)}$ . it ranges from  $100\Omega$  to  $100\text{ k}\Omega$ .

# \* Temperature effect:

⇒ Case (i) :  $V_p$

$V_p$  : dependent on Temp.

: Inc by  $2.2 \text{ mV } ^\circ\text{C}^{-1}$ .

$$T \uparrow \rightarrow V_p \uparrow \rightarrow I_D \uparrow$$

PTC

PTC: +ve Temp. Coefficient.  
(OR)

$$T \uparrow \rightarrow t_{ch} \uparrow \rightarrow R_{ch} \downarrow \rightarrow I_D \uparrow$$

PTC

$$T \uparrow \rightarrow I_D \downarrow$$

NTC

⇒ Case (ii):  $\mu$

$$\mu \propto \frac{1}{T^m} \text{ (or) } \mu \propto T^{-m}$$

Si:  $m = 2.5$  for e<sup>-</sup>.  $\rightarrow \mu_n \propto \frac{1}{T^{2.5}}$

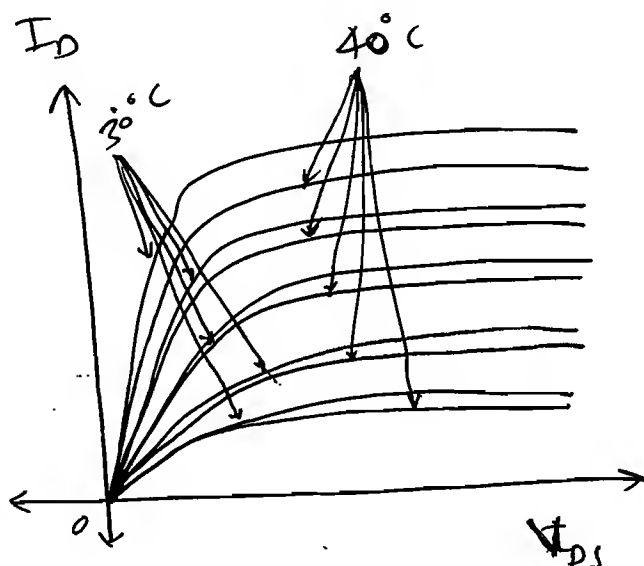
= 2.7 for holes.  $\rightarrow \mu_p \propto \frac{1}{T^{2.7}}$

Ge:  $m = 1.66$  for e<sup>-</sup>.

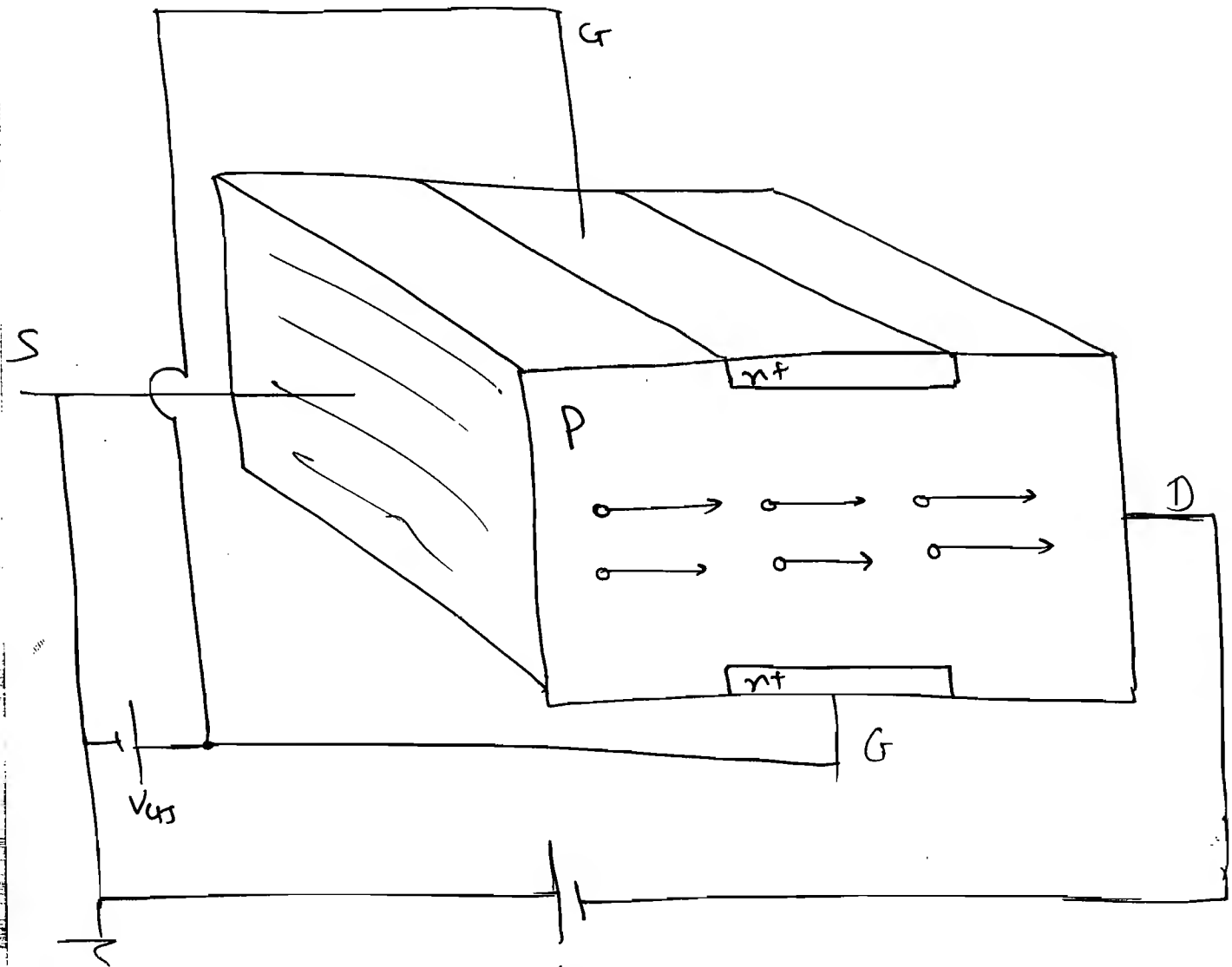
= 2.33 for holes.

$$T \uparrow \rightarrow \mu \downarrow \rightarrow I_D \downarrow$$

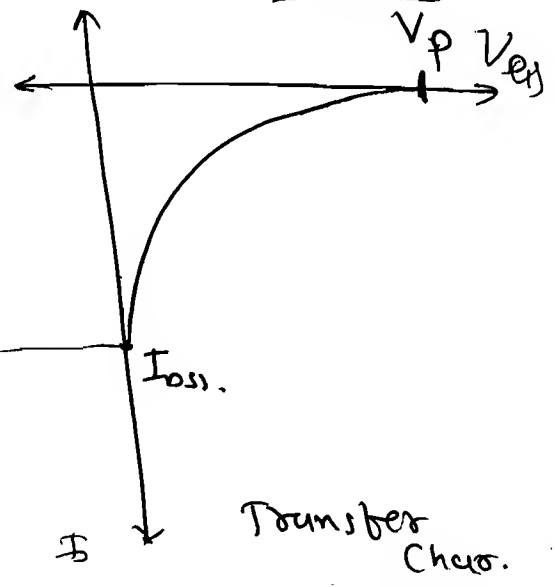
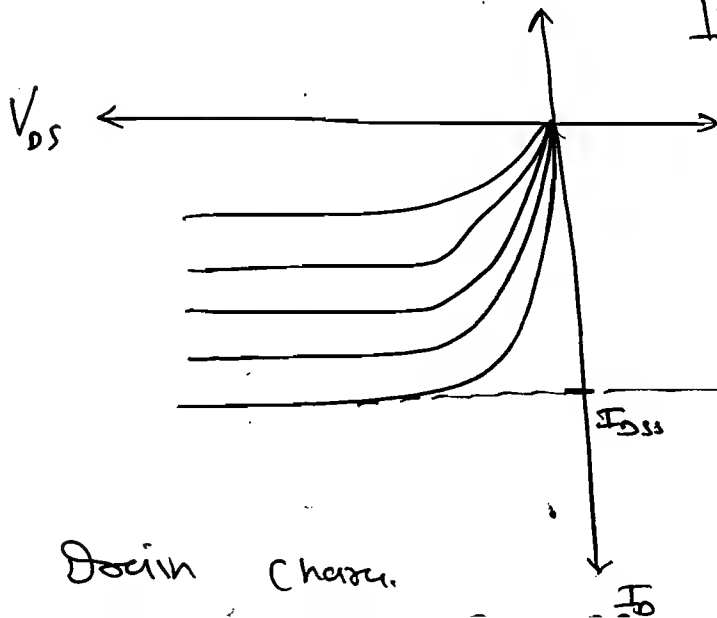
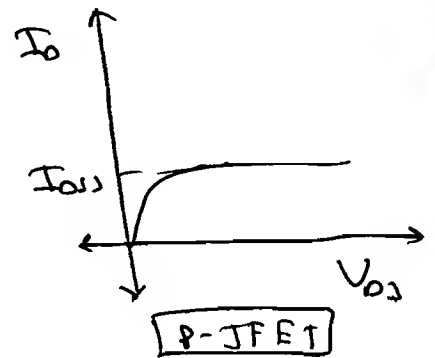
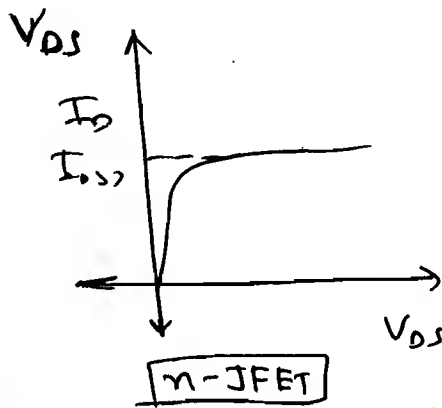
NTC



# \* P-Channel JFET:



$V_{DS} = +ve$   
 $V_{GS} = +ve$   
 $V_P = +ve$



Drain Charac.

Transfer Charac.

$$\Rightarrow V_{DS} = V_{GS} - V_P$$

$\uparrow$              $\uparrow$              $\uparrow$   
 -ve          +ve          +ve.

$$\text{let, } \left. \begin{array}{l} V_P = +10V \\ V_{GS} = 10V \end{array} \right\} V_{GS} = V_P = 10V \left. \vphantom{\begin{array}{l} V_P = +10V \\ V_{GS} = 10V \end{array}} \right\} V_{GS}$$

$$\left. \begin{array}{l} V_P = 10V \\ V_{GS} = 12V \end{array} \right\} V_{GS} > V_P$$

$0 < V_{GS} < V_P \rightarrow \text{Linear (or) Sat.}$

$$V_{GS} - V_P = 2 - 10V = -8V$$

ib  $V_{DS} = -8V$

ib  $V_{DS} = -3V$

$V_{DS} > V_{GS} - V_P \Rightarrow \text{linear region.}$

for  $V_{DS} < V_{GS} - V_P \Rightarrow \text{Sat. region.}$

\* Imp Points to be Remember for P-JFET:

$\Rightarrow$  P-channel JFET operates with +ve gate

Voltages i.e. +ve  $V_{GS}$  values.

$\Rightarrow$  Gate to Source Voltage ( $V_{GS}$ ) and pinch-off Voltages ( $V_P$ ) are +ve for P-JFET.

$\Rightarrow$  P-JFET operates in depletion mode for +ve  $V_{GS}$  values.

$\Rightarrow$  In P-JFET as  $V_{GS}$  increases pinch-off happens for higher values of  $V_{GS}$ .

$\Rightarrow$  Condition for pinch-off (or) Sat.

$$V_{DS} = V_{GS} - V_p$$

$\uparrow$        $\uparrow$        $\uparrow$   
 -ve      +ve      +ve

$\Rightarrow$  In p-channel JFET as  $V_{GS}$  increases Avalanche - Breakdown happens due to avalanche effect for higher values of  $V_{DS}$ .

$\Rightarrow$  For  $V_{GS} \geq V_p$  p-channel JFET operates in cut-off region and its drain current  $I_D = 0$ .

$\Rightarrow$  For  $0 < V_{GS} < V_p$  &  $V_{DS} > V_{GS} - V_p$  it operates in linear region and its drain current,

$$I_D = \frac{2 I_{DSS}}{V_p^2} \left[ (V_{GS} - V_p) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$\uparrow$        $\uparrow$        $\uparrow$   
 +ve      +ve      -ve

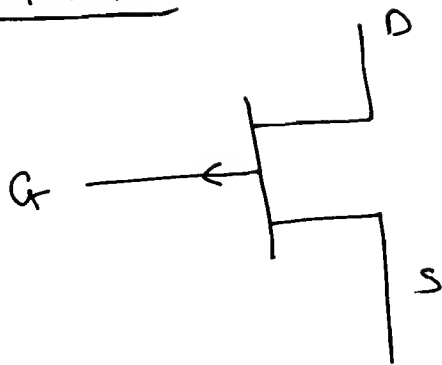
$\Rightarrow$  For  $0 < V_{GS} < V_p$  &  $V_{DS} < V_{GS} - V_p$ , it operates in ~~linear~~ saturation region and its drain current,

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_p} \right]^2$$

$\uparrow$        $\uparrow$   
 +ve      +ve

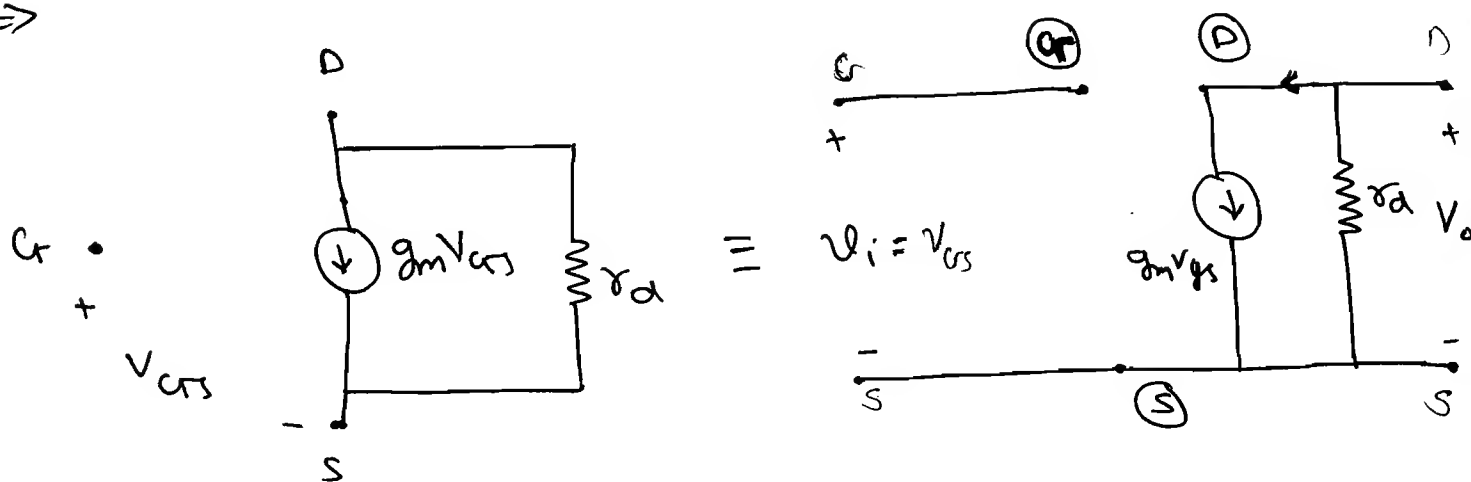


\* Symbol :

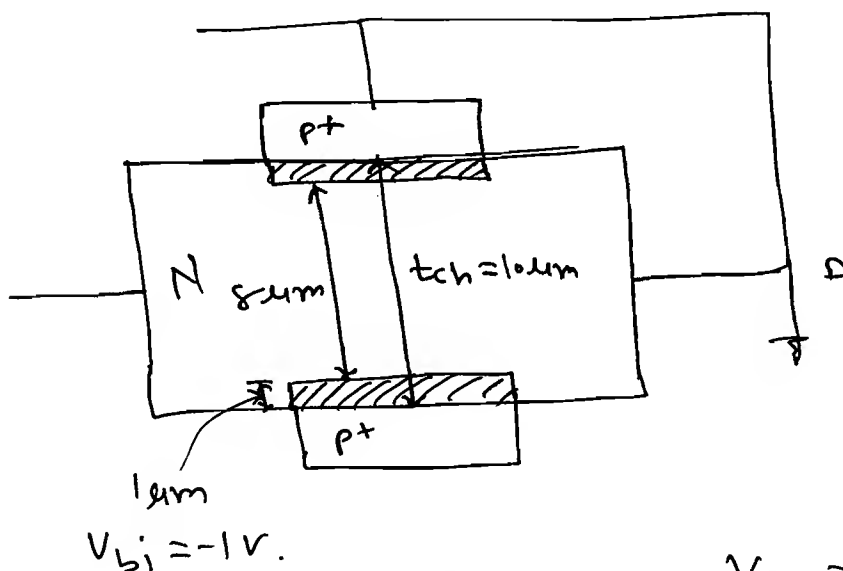


\* Small signal equivalent ckt (or) AC equivalent ckt.

⇒



Q



Channel resistance when  $V_{gs} = 0V$ .  
 $R_{ch} = 600 \Omega$  when  $t_{ch} = 10 \mu m$ .  
 $R_{ch} = ?$  when  $t_{ch} = 8 \mu m$ .

Soln:

$$R_{ch1} = \frac{SL}{w \times t_{ch1}}, \quad R_{ch2} = \frac{SL}{w \times t_{ch2}}.$$

$$\therefore \frac{R_{ch1}}{R_{ch2}} = \frac{t_{ch2}}{t_{ch1}}$$

$$\therefore R_{ch2} = \frac{t_{ch1}}{t_{ch2}} \times R_{ch1}$$

$$= \frac{10}{8} \times 600$$

$$\boxed{R_{ch2} = 750 \Omega}$$

**Q-10** The channel Resistance when  $V_{GS} = -3V$ .

Soln:

$$V_j = \frac{e N_D}{2\epsilon} \cdot \omega^2$$

$$\therefore V_j \propto \omega^2$$

$$\text{When } V_{GS} = 0$$

$$V_j = V_{\phi} = -1V = V_{bi}$$

$$\text{When } V_{GS} = -3$$

$$V_j = V_{\phi} + V_{\text{eff}} = -1 - 3 = -4V$$

$$\omega = 1 \mu m \quad \text{When } V_{GS} = 0.$$

$$\therefore \frac{V_{j1}}{V_{j2}} = \left( \frac{\omega_1}{\omega_2} \right)^2$$

$$\therefore \frac{1}{1} = \omega_2^2 = \frac{V_{j2}}{V_{j1}} \times \omega_1^2$$

$$\therefore \omega_2^2 = \frac{-4}{-1} \times (1 \mu m)^2$$

$$\therefore \boxed{\omega_2 = 2 \mu m}$$

$$\therefore \text{Now, } t_{ch3} = 10 - 2 - 2 = 6 \mu m.$$

$$\therefore \frac{R_{ch3}}{R_{ch1}} = \frac{t_{ch1}}{t_{ch3}}$$

$$\therefore R_{ch3} = \frac{10}{6} \times 600$$

$$\boxed{R_{ch3} = 1000 \Omega}$$

$$P_D = V_{SD} \cdot I_D$$

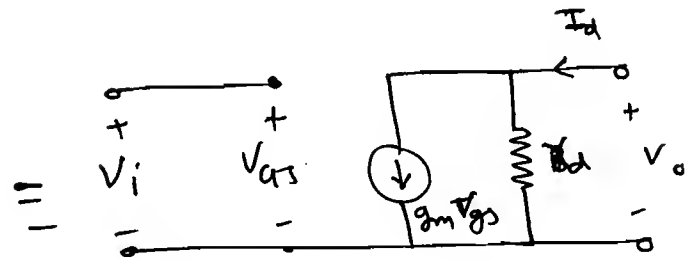
Stable than BTT as  
coefficient.

For JFET: [bc analysis]

- ① Fixed biased.
- ② Self biased.
- ③ Voltage divider

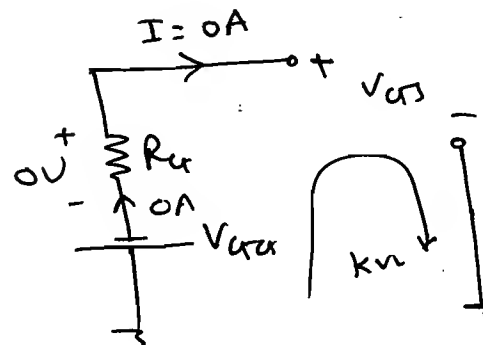
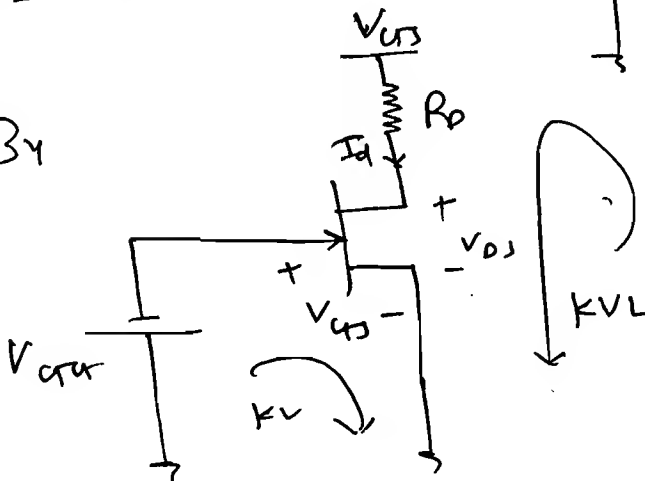
biased.

① Fixed biased:



$$\Rightarrow V_{DS} = V_D - V_S$$

$$V_{as} = V_a - V_s$$


$$\Rightarrow B_4$$


$$\Rightarrow \text{By KVL } -V_{GS} - V_{DS} = 0.$$

$$\therefore \boxed{V_{GS} = -V_{DS}} \quad \checkmark$$

$$\Rightarrow I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$$

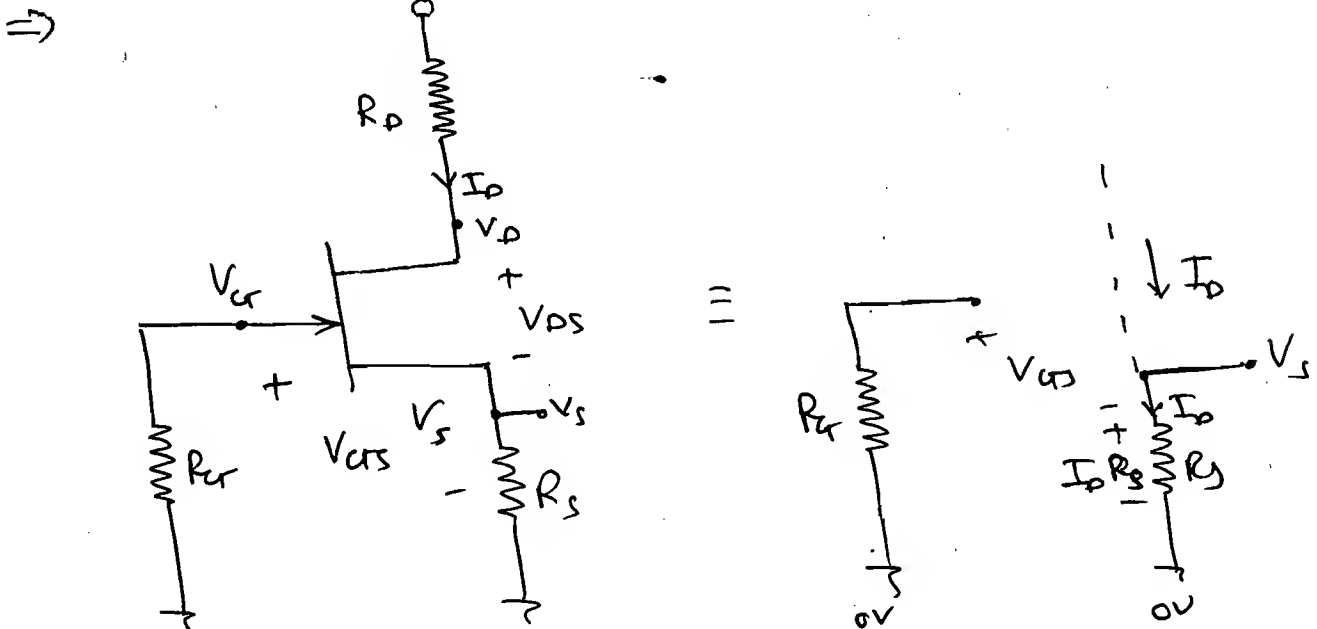
$$\therefore \boxed{I_D = I_{DSS} \left[ 1 + \frac{V_{DS}}{V_P} \right]^2} \quad \checkmark$$

$$\Rightarrow \text{By KVL,}$$

$$V_{DD} - I_D R_D - V_{DS} = 0.$$

$$\therefore \boxed{V_{DS} = V_{DD} - I_D R_D} \quad \checkmark$$

② Self-biased :



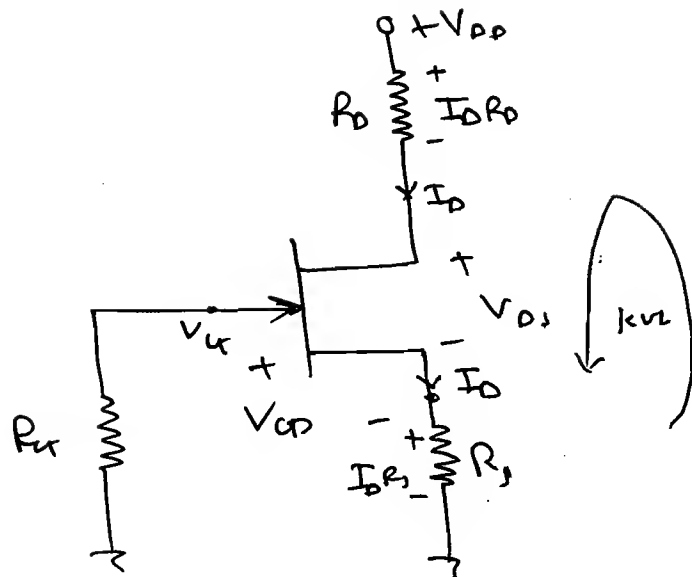
$$\Rightarrow V_{GS} = V_G - V_S$$

$$\text{By, KVL } 0 - V_{GS} - I_D R_S = 0$$

$$\Rightarrow \boxed{V_{GS} = -I_D R_S} \quad \checkmark$$

$$V_{DS} = V_D - V_S.$$

$\Rightarrow$



$\Rightarrow$  By, KVL,  $V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0.$

$\therefore V_{DS} = V_{DD} - I_D (R_D + R_S).$

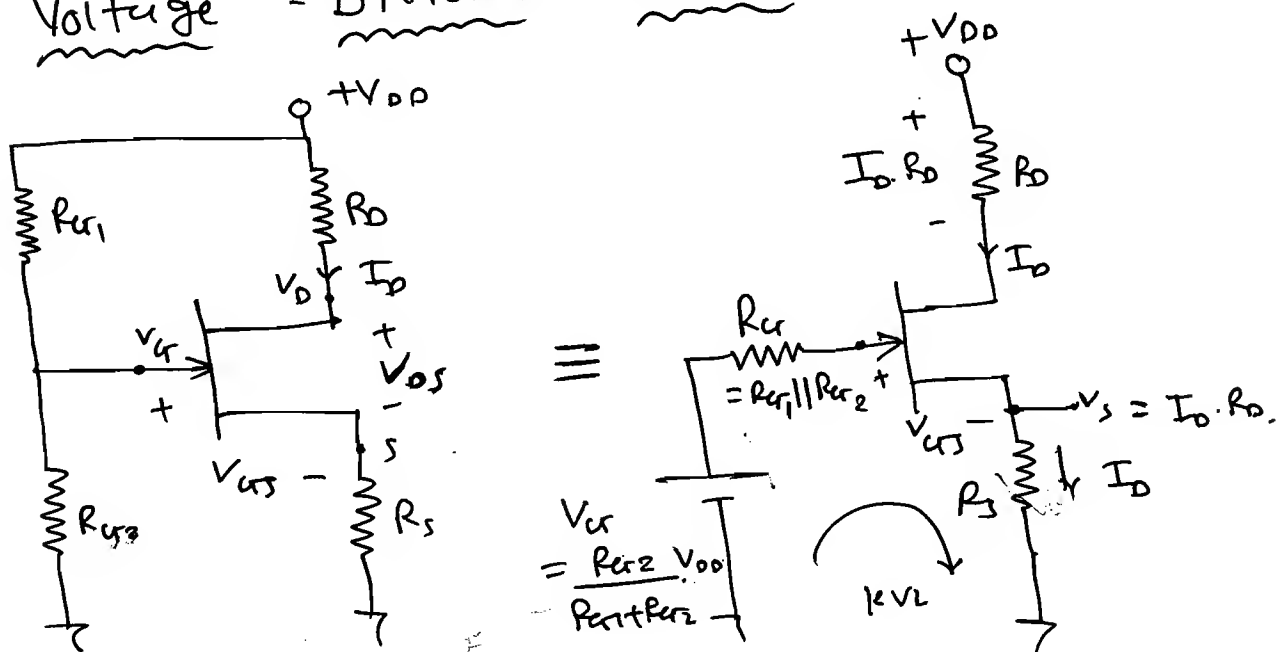
But,  $I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$

$V_{GS} = -I_D R_S$

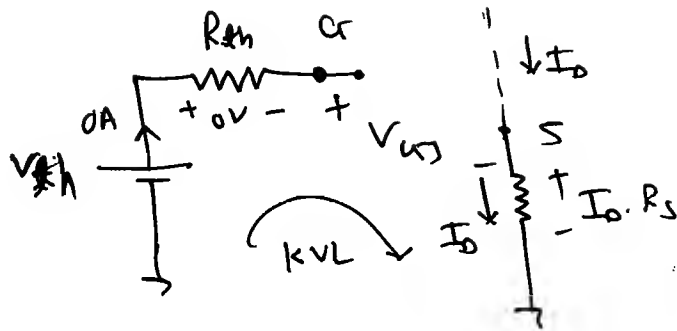
$\therefore I_D = I_{DSS} \left[ 1 + \frac{I_D R_S}{V_P} \right]^2$

$\therefore V_{DS} = V_{DD} - I_{DSS} \left[ 1 + \frac{I_D R_S}{V_P} \right]^2 (R_D + R_S)$

③ Voltage Divider biased:



$$\Rightarrow V_{GS} = V_G - V_S$$



$$\Rightarrow V_G = V_{th} + 0$$

$$V_G = V_{th}$$

$$V_G - V_{GS} - I_D R_S = 0.$$

$$\therefore \boxed{V_{GS} = V_G - I_D R_S}$$

$$V_G = V_{th} = \frac{R_{G2}}{R_{G1} + R_{G2}} \times V_{DD}$$

$$\Rightarrow I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$$

$$\therefore \boxed{I_D = I_{DSS} \left[ 1 - \frac{V_G - I_D R_S}{V_P} \right]^2}$$

$$\Rightarrow V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$\therefore \boxed{V_{DS} = V_{DD} - I_D (R_D + R_S)}$$

Now,  $V_{GS}$  should be -ve.

$$\text{So, } I_D R_S > V_G$$

$$\frac{V_{DS} - V_{DD}}{R_D + R_S} \cdot R_S > V_G$$

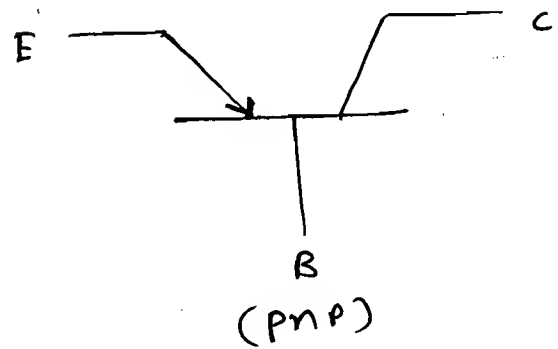
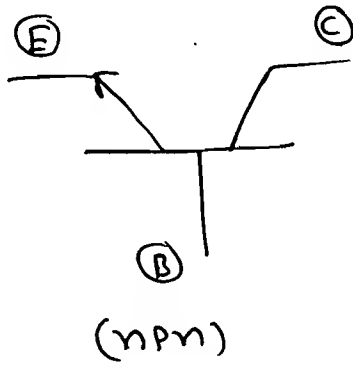
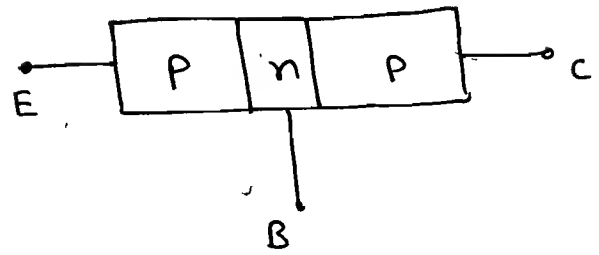
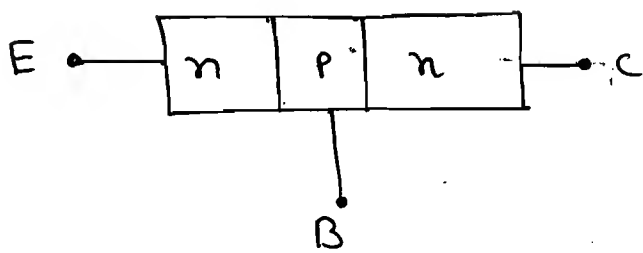
Select  $R_D$  &  $R_S$  in such a way

$$\text{that } I_D R_S > V_G \Rightarrow V_{GS} = -ve.$$

# ☆ Amplifier Analysis: (Ac Analysis):

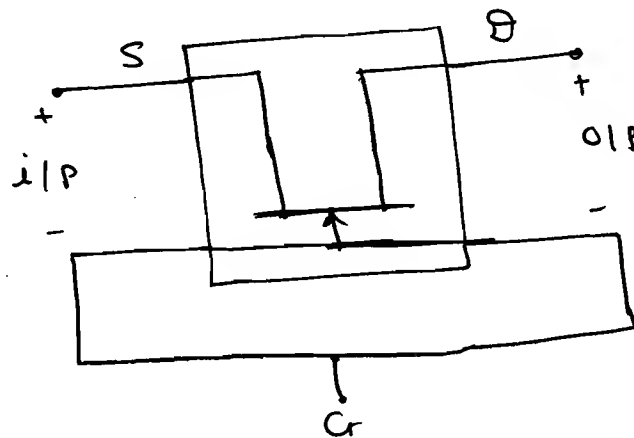
24)

⇒

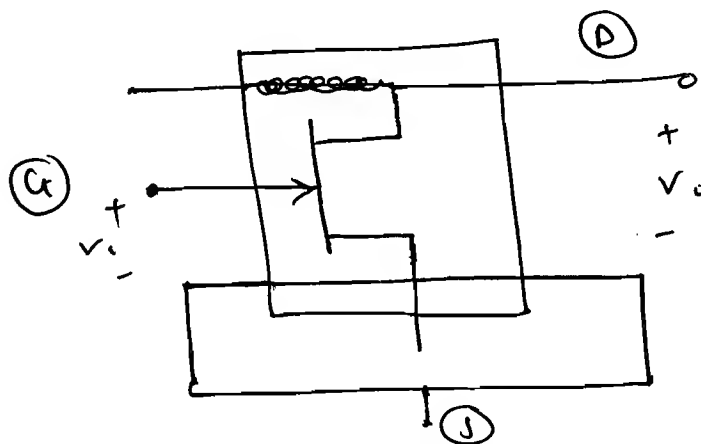


⇒ Configuration of JFET:

① Common gate configuration:



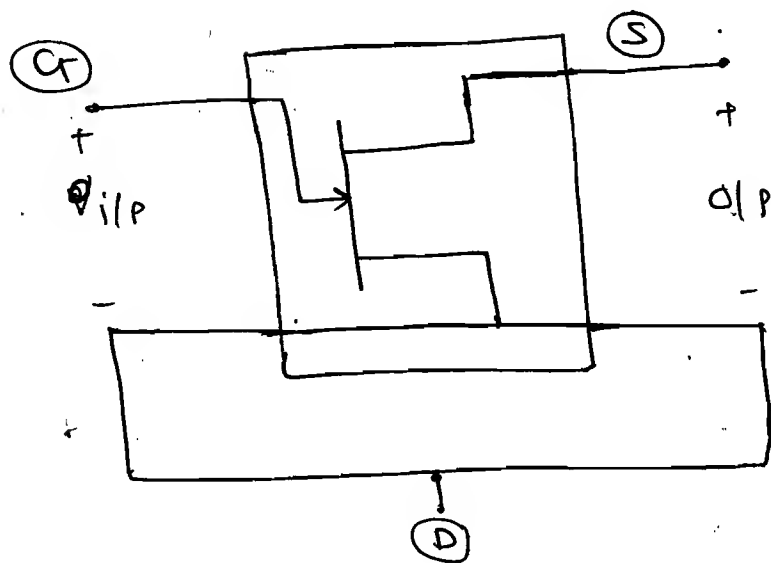
② Common source configuration:



Note:

(3)

## Common Drain Configuration:



(Source follower)

Note:

⇒ CD and CS can not be used as the current amplifiers. because FET has high input impedance and o/p impedance. i.e. at input it is open ckt. Therefore no input current. As in CD and CS input is given to the gate and when i/p is given to gate it is open ckt. and they can be not be used as current amplifiers. In common gate  $I_D = I_S$  so, current gain is 1. i.e. no amplification.

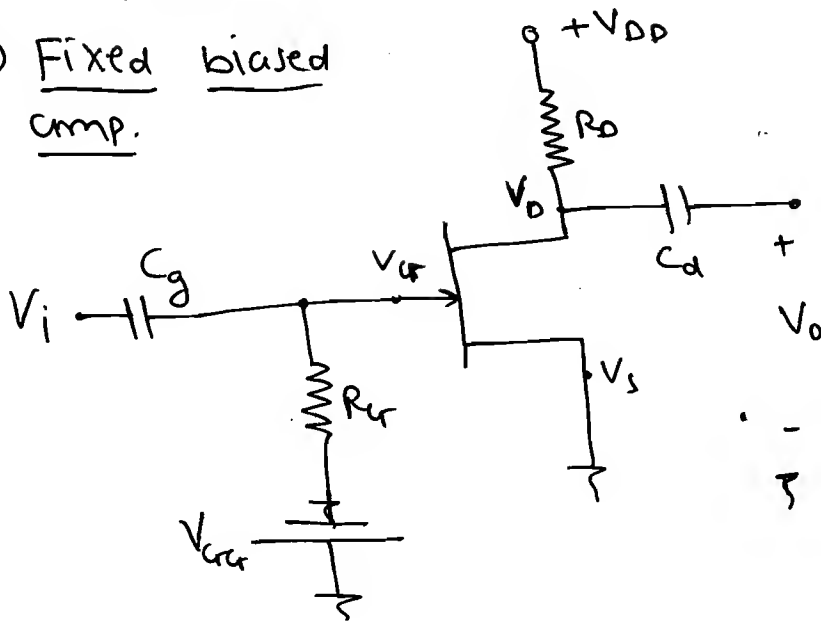
$$A_{Icr} = \frac{I_o}{I_i} = \frac{I_o}{I_S} = 1.$$

No current amplification.



# ① Common Source Configuration Amplifier. <sup>25)</sup>

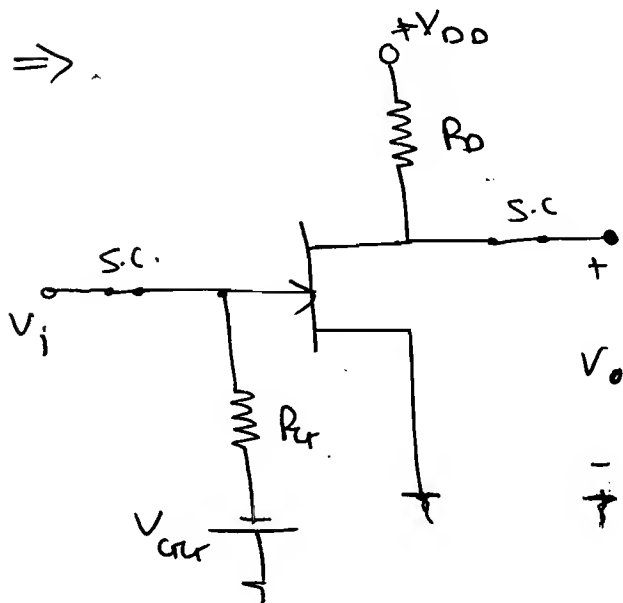
## (1) Fixed biased Comp.



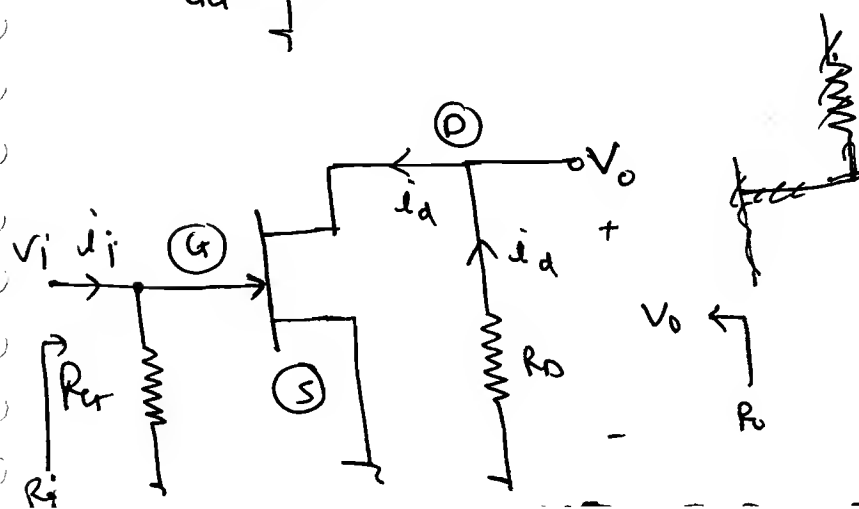
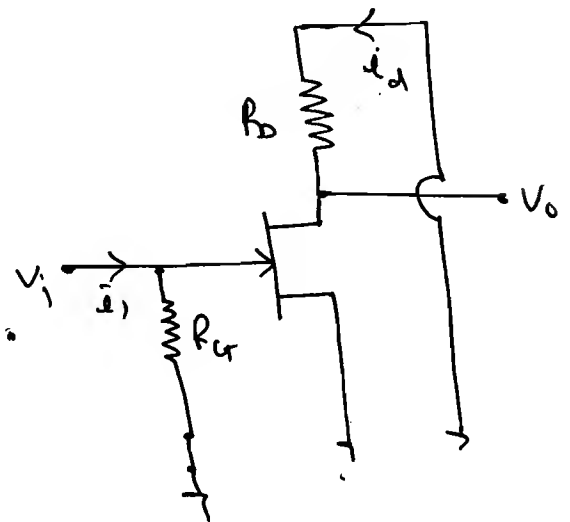
Steps:

- ① Short ckt the capacitance.
- ② Short ckt the d.c. power supply to ground.
- ③ Identify the terminals of JFET.
- ④ Replace JFET with its eq<sup>n</sup> ckt.

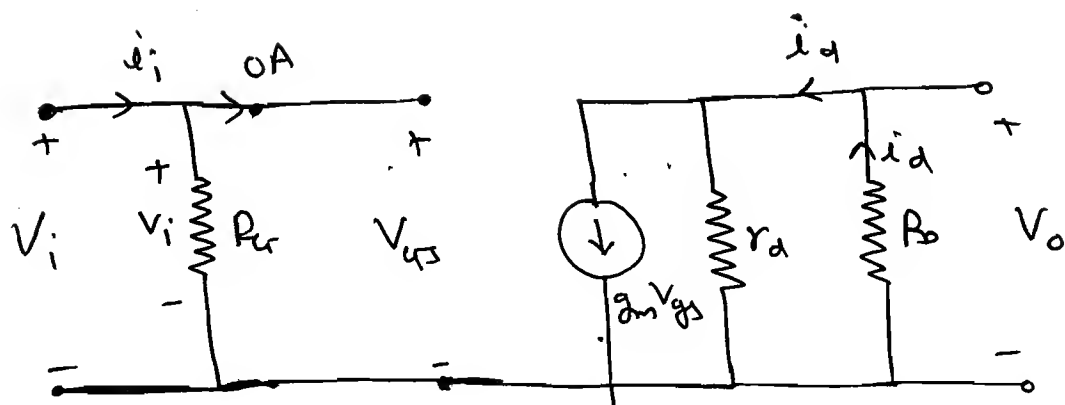
⇒



=



eqn ckt:



Small signal eqn ckt (o<sub>2</sub>)  
h-parameter eqn ckt (o<sub>2</sub>)  
Ac eqn ckt.

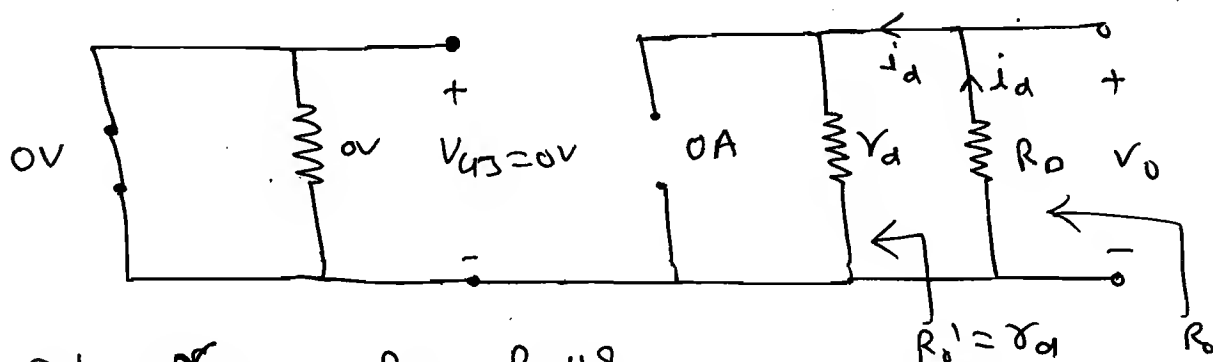
① Input Resistance (R<sub>i</sub>):

⇒ Input resistance  $R_i = \frac{v_i}{i_i} = \frac{i_x \cdot R_G}{i_i} = R_G.$

∴  $R_i = R_G$

② Output Resistance (R<sub>o</sub>):

⇒ for finding R<sub>o</sub> make d.c. = 0.



⇒  $R_o' = r_d, R_o = R_D || r_d.$

∴  $R_o = R_D || r_d.$

ideally  $r_d = \infty.$

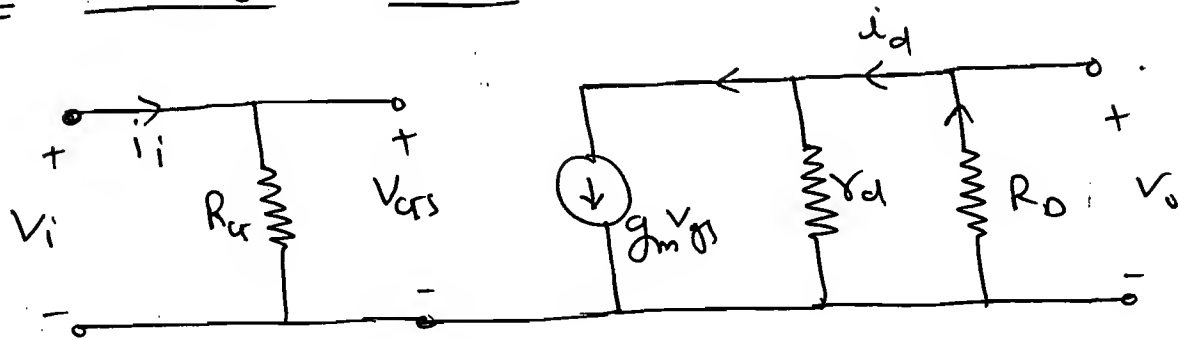
Practically  $r_d = 50k$  to  $100k$

So, for  $r_d \gg R_D$ . (or)  $r_d \geq 10R_D$ .

26)

$$\therefore R_0 \approx R_D$$

③ Voltage gain:



$$\therefore V_i = R_r \cdot i_i = V_{gs}$$

$$\therefore V_o = -g_m V_{gs} \cdot [r_d \parallel R_D]$$

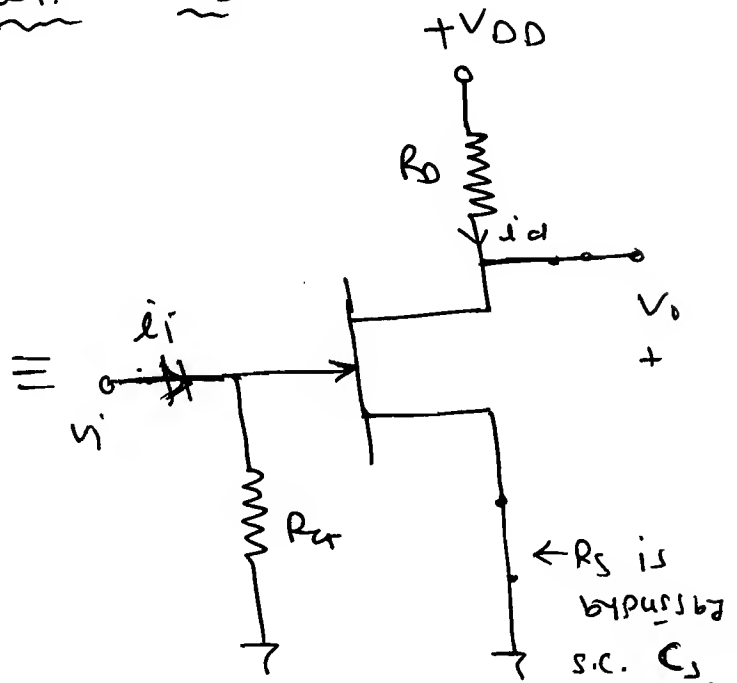
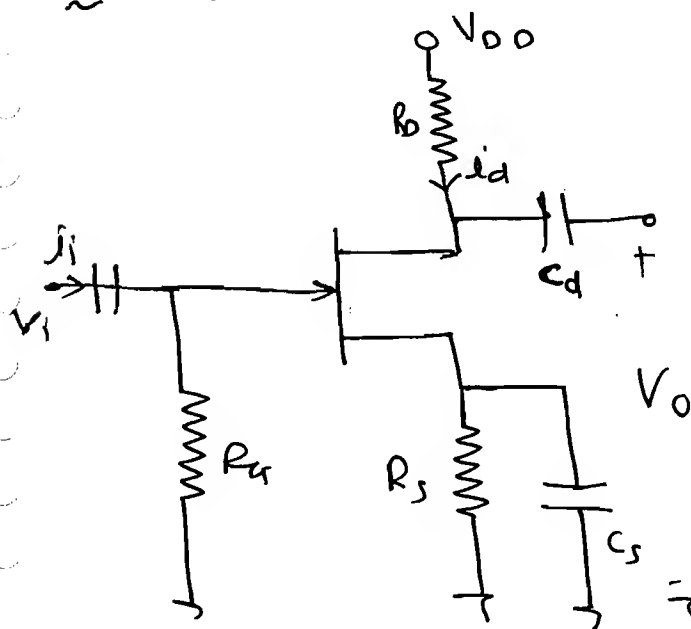
$$\therefore A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs} [r_d \parallel R_D]}{V_{gs}}$$

$$\therefore A_v = -g_m [r_d \parallel R_D]$$

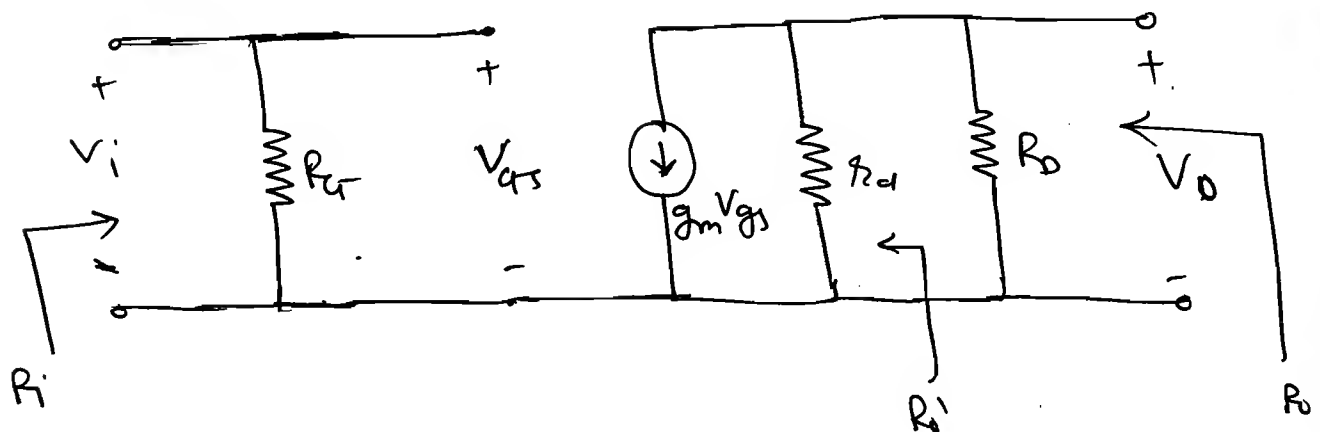
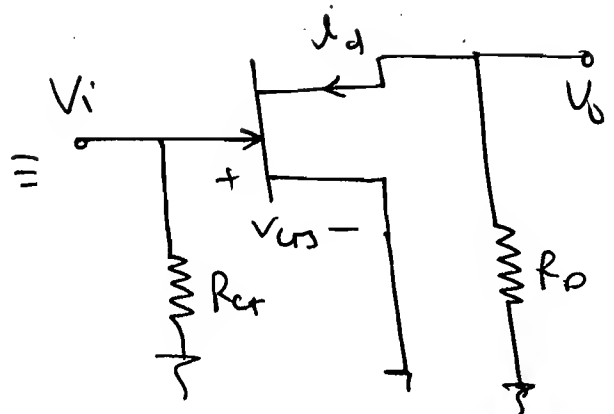
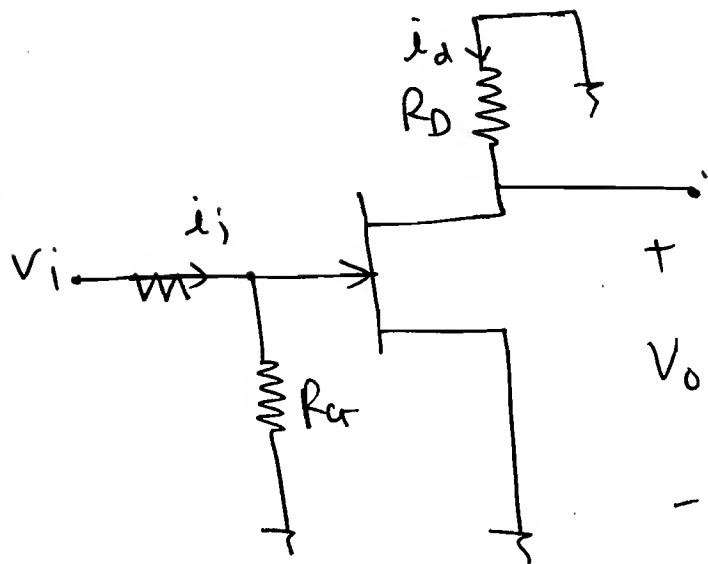
$$\text{But } r_d \gg R_D \Rightarrow r_d \parallel R_D \approx R_D$$

$$\therefore A_v = -g_m R_D$$

② Self bias comp. (with  $C_s$ ):



$\Rightarrow$



① Input Resistance:

$\Rightarrow$  Input Resistance  $R_i = R_{cr}$

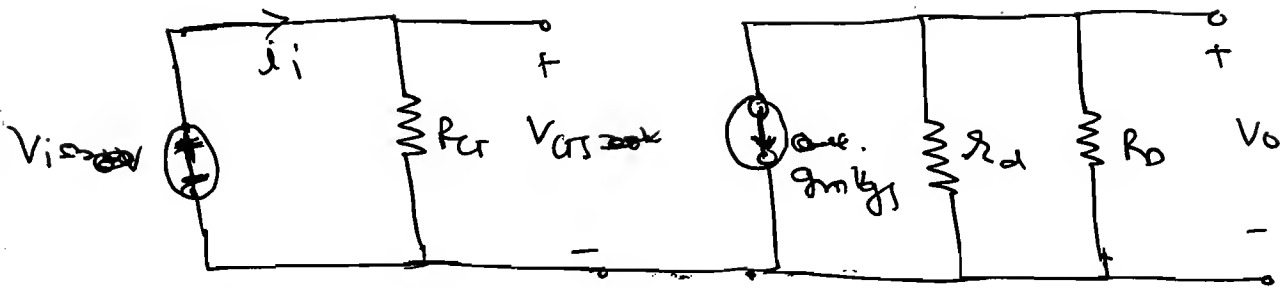
② Output Resistance:

$\Rightarrow R_o' = R_d, R_o = R_d \parallel R_D$

$\therefore R_o = R_d \parallel R_D$   
 $R_o \approx R_D (\because R_d \gg R_D)$

### ③ Voltage gain:

277



$$\therefore V_{gs} = V_i$$

$$\therefore V_o = -g_m V_{gs} [r_d || R_o]$$

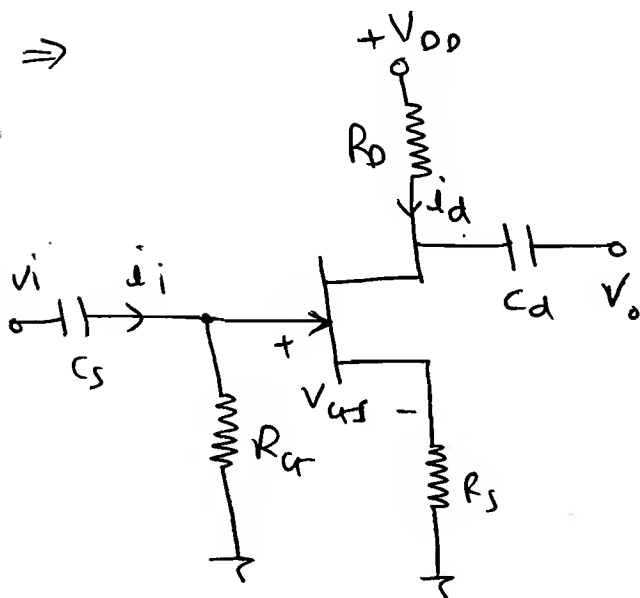
$$\therefore A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs} [r_d || R_o]}{V_{gs}}$$

$$\therefore \boxed{A_v = -g_m [r_d || R_o]}$$

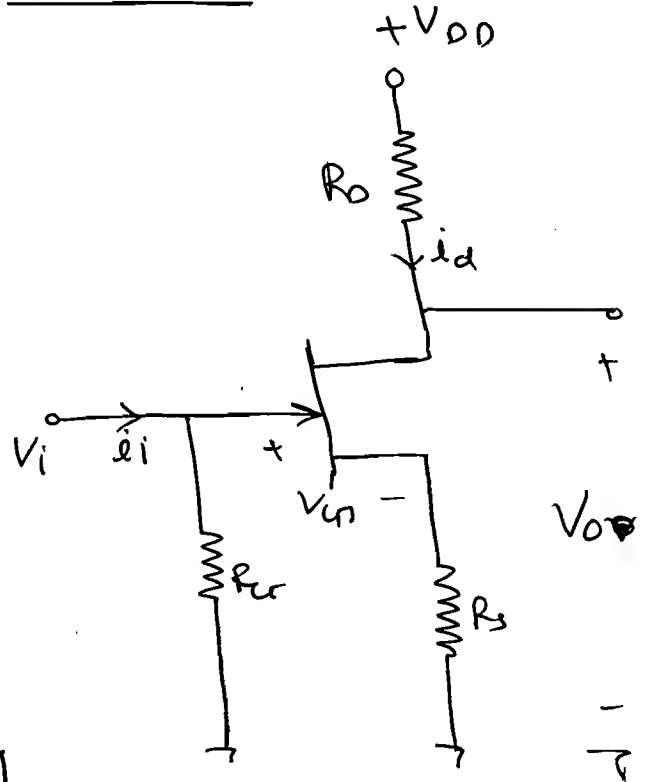
$$\boxed{A_v \approx -g_m R_o. (\because r_d \gg R_o)}$$

### ③ Self biased amp. (without $C_s$ ):

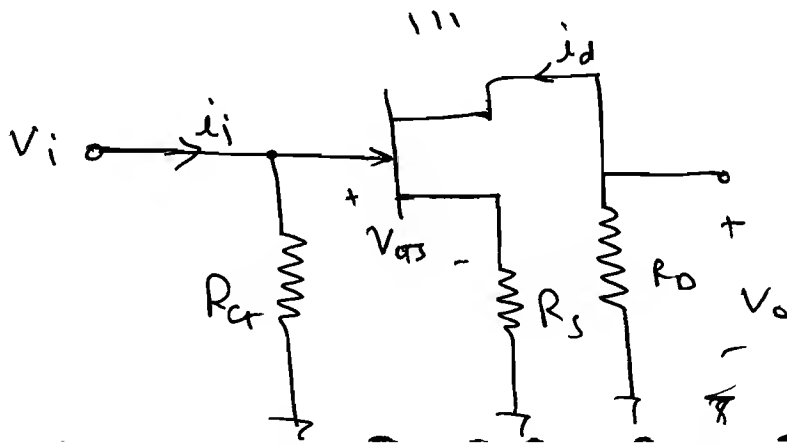
$\Rightarrow$

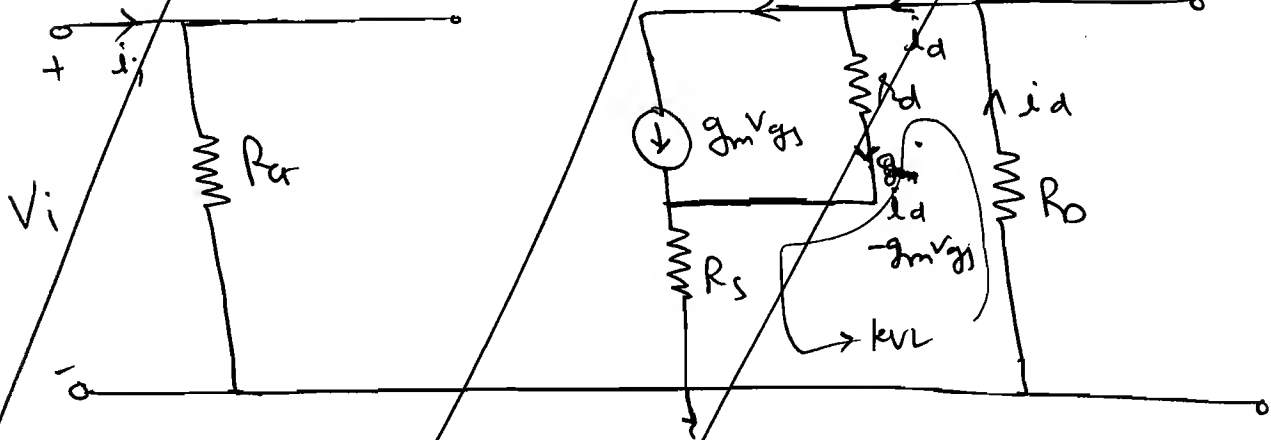
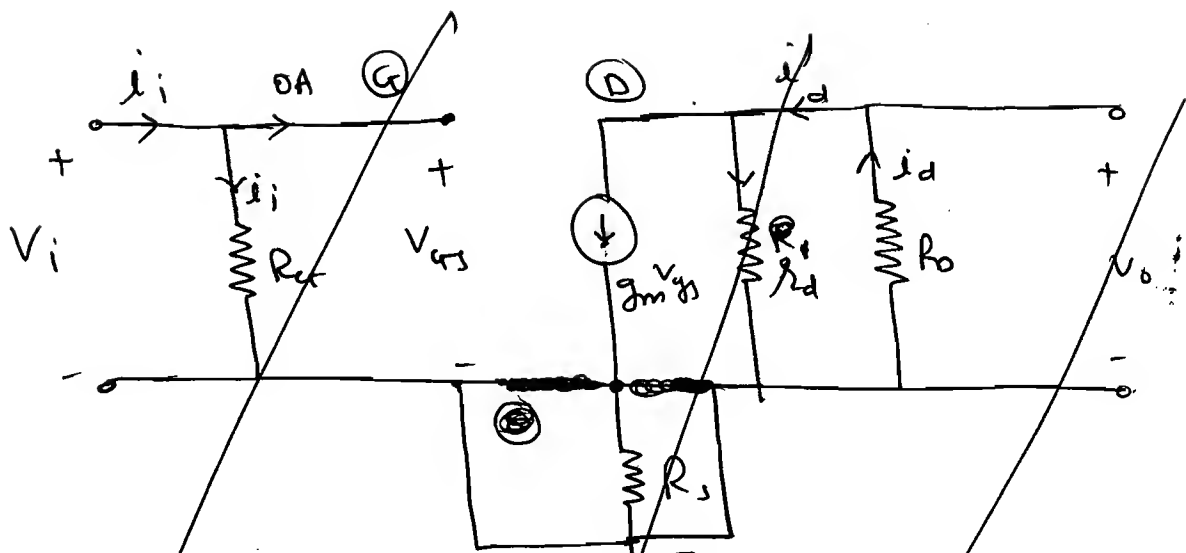


$\equiv$



$\Rightarrow$





By KVL

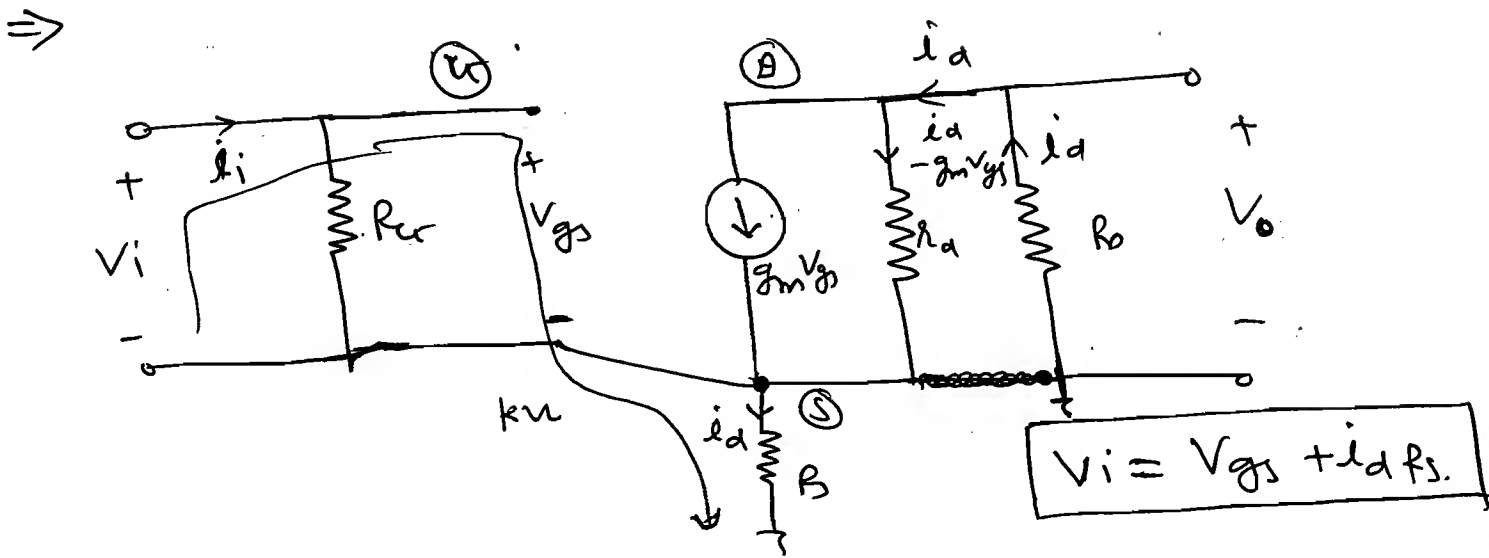
① Input

Resistance ( $R_i$ ):-

⇒

$$R_i = R_d$$

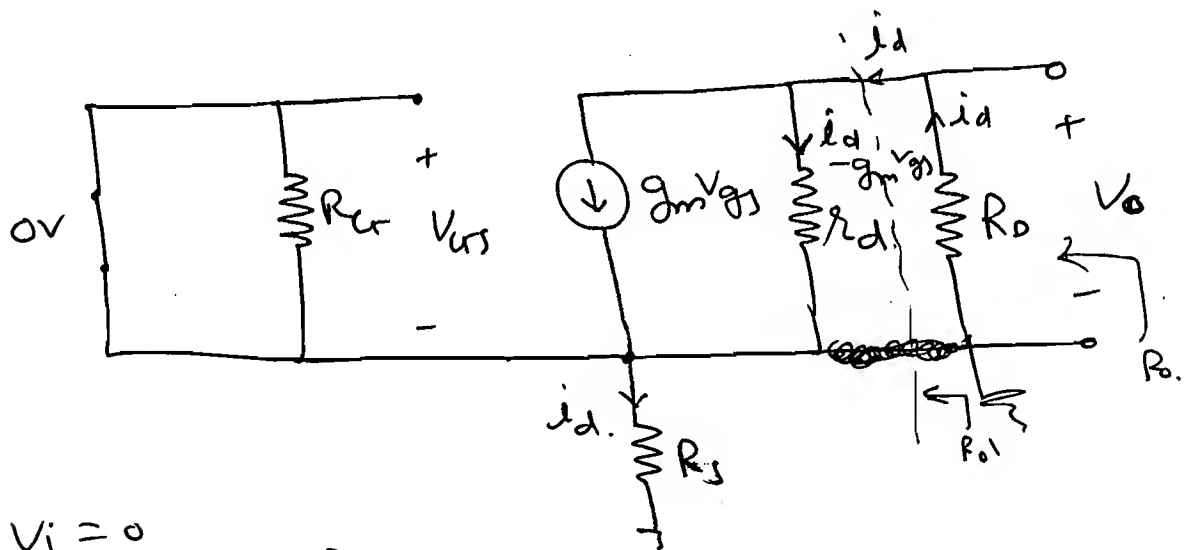
②



① Input Resistance ( $R_i$ ):

⇒ Input Resistance  $R_i = R_{cr}$

② Output Resistance ( $R_o$ ):



By KVL,  $V_o = r_d (i_d - g_m V_{gs}) + R_s i_d$

$R_o = R_D || R_o'$

$R_o' = \frac{V_o}{i_d}$

∴  $\frac{V_o}{i_d} = R_o' = r_d (1 + g_m R_s) + R_s$

$R_o' = r_d + (1 + g_m r_d) R_s$

$$R_o = R_o \parallel [r_d + (1 + \mu)R_s]$$

$$(\because \mu = g_m r_d)$$

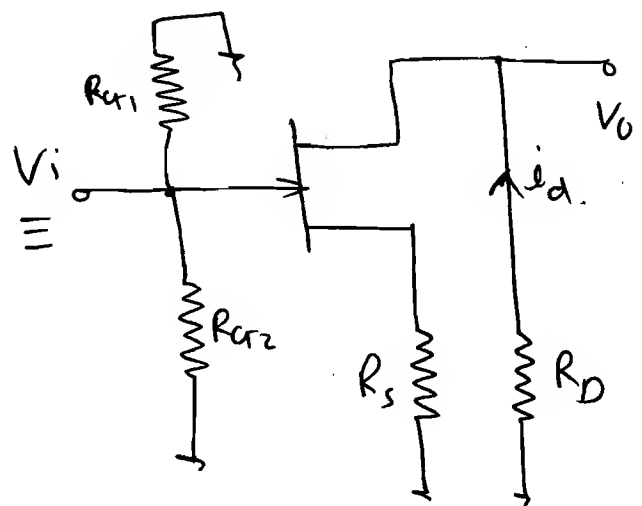
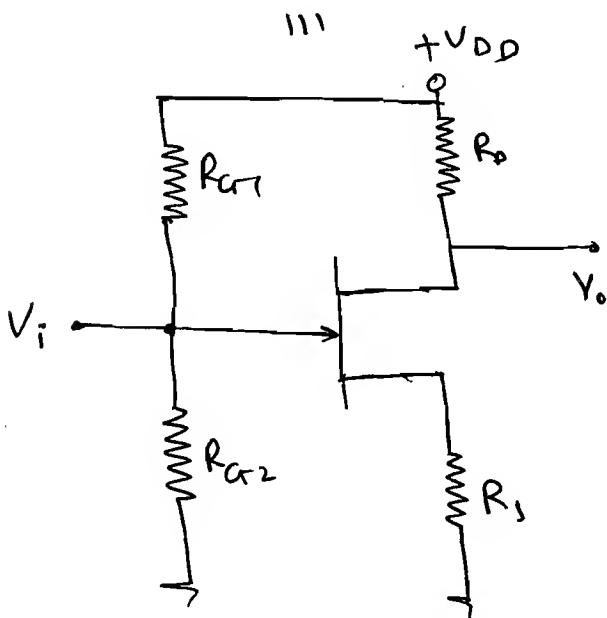
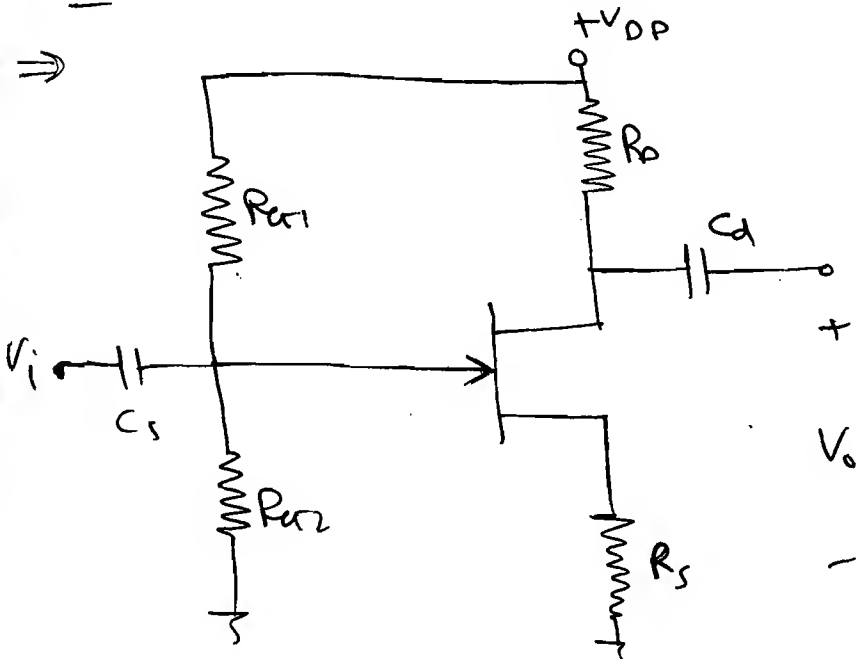
③ Voltage gain: ( $A_v$ ):

$$V_i = V_{gs} + i_d R_s$$

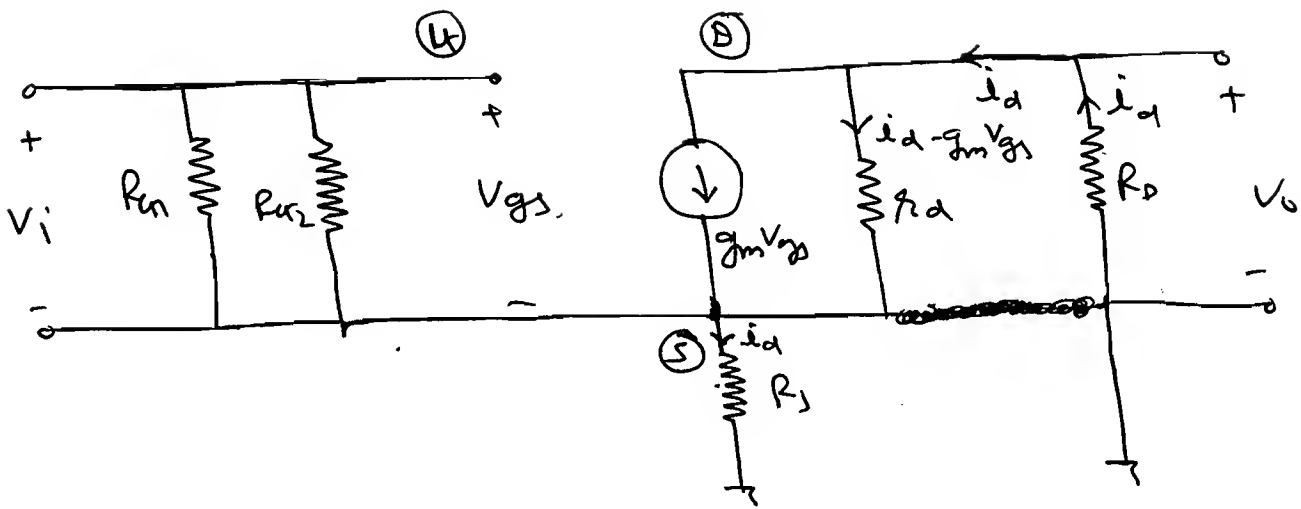
$$V_{gs} = V_i - i_d R_s$$

$$A_v = \frac{-g_m R_o}{1 + g_m R_s}$$

④ Voltage divider bias amp (without  $C_s$ ):







① Input Resistance ( $R_i$ ):

$$\Rightarrow R_i = R_{n1} \parallel R_{r2}$$

② Output Resistance ( $R_o$ ):

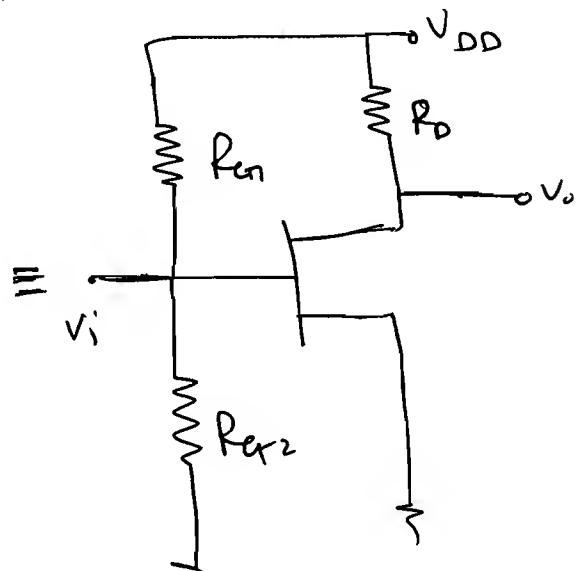
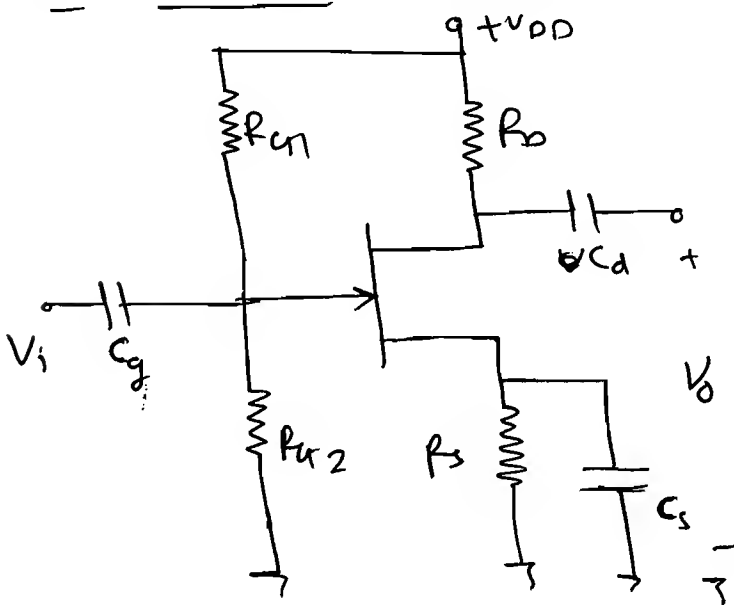
$$\Rightarrow R_o = R_{r1} \parallel [r_o + (1 + \mu) R_s]$$

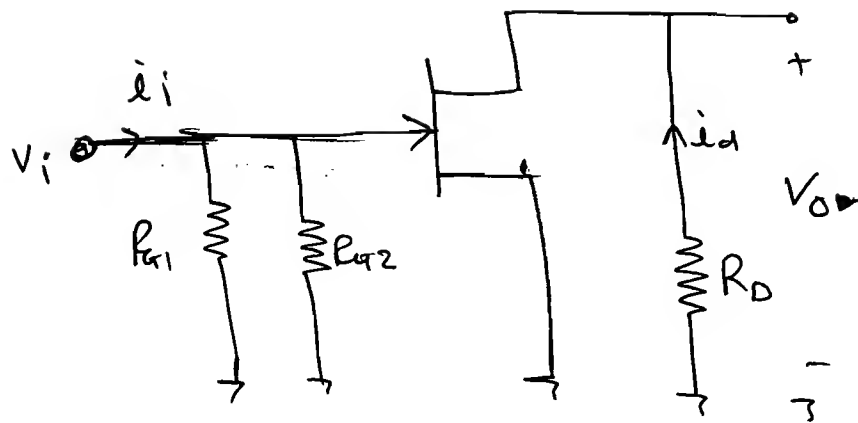
( $\because \mu = g_m r_o$ )

③ Voltage gain: ( $A_v$ ):

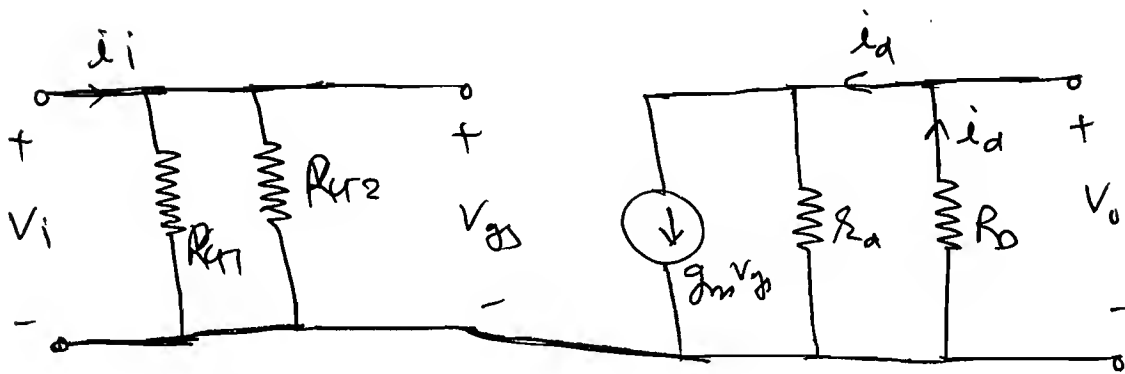
$$\Rightarrow A_v = \frac{-g_m R_o}{1 + g_m R_s}$$

⑤ Voltage divider bias (with  $C_s$ ):





|||



① Input Resistance:

$$\Rightarrow R_i = R_{g1} \parallel R_{g2}$$

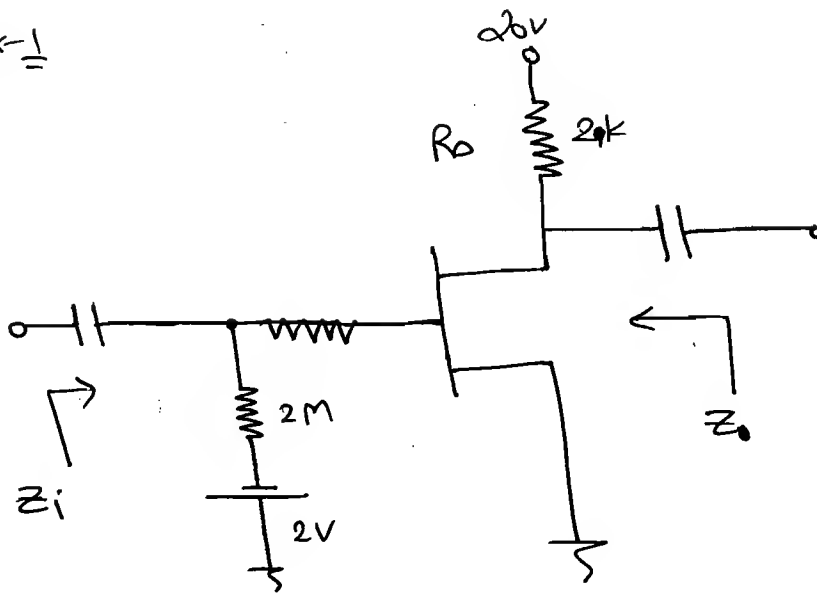
② Output Resistance ( $R_o$ ):

$$\Rightarrow R_o = R_D \parallel R_L \approx R_D \quad (\because R_L \gg R_D)$$

③ Voltage gain ( $A_v$ ):

$$\Rightarrow A_v = -g_m (R_D \parallel R_L)$$

$$\therefore A_v = -g_m R_D$$

Ex-1

$$R_d = 20k$$

$$I_{DSS} = 10mA$$

$$V_p = -8V$$

$$\underline{Q-10} \quad Z_i \approx R_i = 2M\Omega$$

$$Z_o = R_d \parallel R_d = \frac{2k}{2} \parallel 20k = \frac{40}{22} = \frac{20}{11} k\Omega$$

Q-11

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_p} \right]^2$$

$$I_D = 10mA \left[ 1 - \frac{-2}{-8} \right]^2$$

$$\boxed{I_D = 5.625mA}$$

$$\begin{aligned} V_{DS} &= V_{DD} - I_D R_d \\ &= 20V - 5.625mA \times 20k \\ V_{DS} &= 8.75V \end{aligned}$$

Q-12

$$g_m = \left| \frac{2I_{DSS}}{-V_p} \right| \left[ 1 - \frac{V_{GS}}{V_p} \right]$$

$$\therefore g_m = \frac{2 \times 10mA}{8} \times \left[ 1 - \frac{-2}{-8} \right]$$

$$\therefore \boxed{g_m = 1.875 \text{ mA/V}}$$

Q-13

$$A_v = -g_m (R_d \parallel R_d)$$

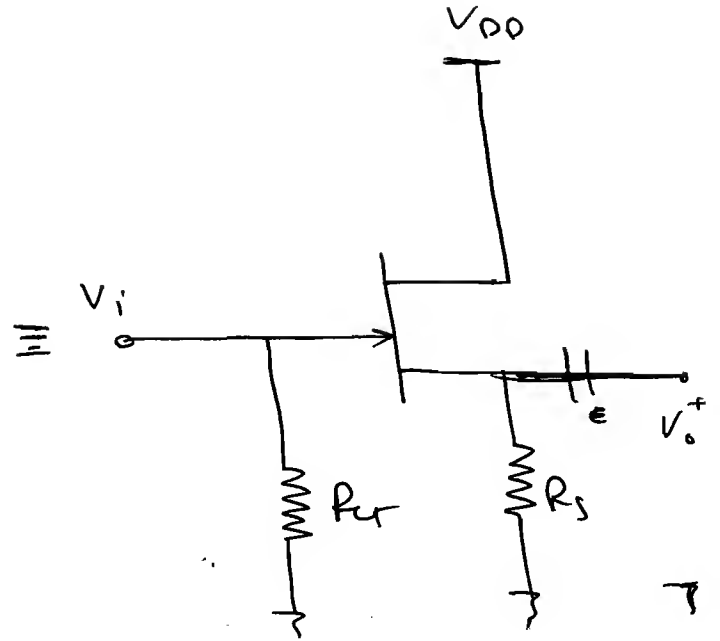
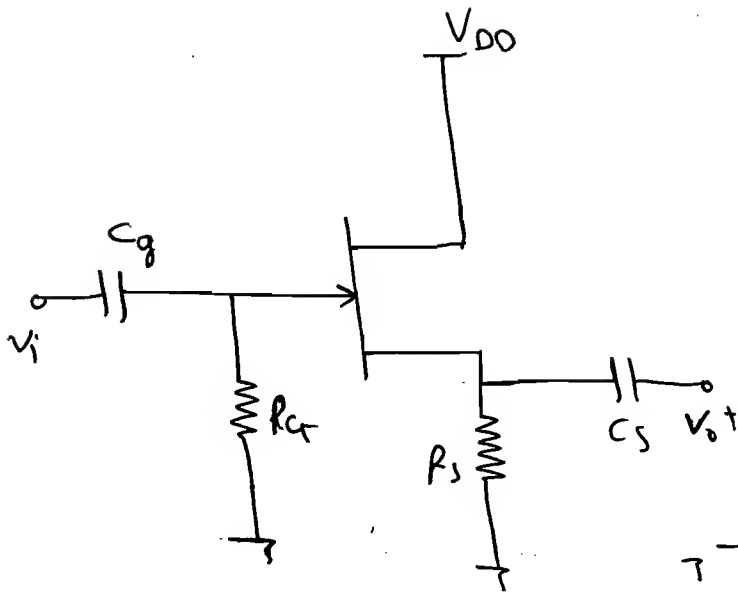
$$A_v = -1.875m \left( \frac{20k}{11} \right)$$

$$\boxed{A_v = -3.4}$$

Parameters	Fixed bias amp	Self bias amp		Voltage divider amp.	
		with $C_S$	without $C_S$	with $C_S$	without $C_S$
1. $R_i$	$R_i = R_G$	$R_i = R_G$	$R_i = R_G$	$R_i = R_{G1}    R_{G2}$	$R_i = R_{G1}    R_{G2}$
2. $R_o$	$R_o = R_D    R_{D2}$ $R_o \approx R_D$	$R_o = R_D    R_{D2}$ $\approx R_D$	$R_D    [R_{D2} + (1+\mu)R_S]$	$R_{D1}    R_D$ $\approx R_D$	$R_D    [R_{D2} + (1+\mu)R_S]$
3. $A_v$	$-g_m (R_D    R_{D2})$ $\approx -g_m R_D$	$-g_m (R_D    R_{D2})$ $= -g_m R_D$	$\frac{-g_m R_D}{1 + g_m R_S}$	$-g_m R_D$	$\frac{-g_m R_D}{1 + g_m R_S}$

## ② Common Drain Amplifier:

### ① Self biased:



$$\Rightarrow R_i = R_{cr}$$

$$R_o = R_d \parallel R_s \parallel \frac{1}{g_m}$$

$$\text{if } R_d \gg R_s$$

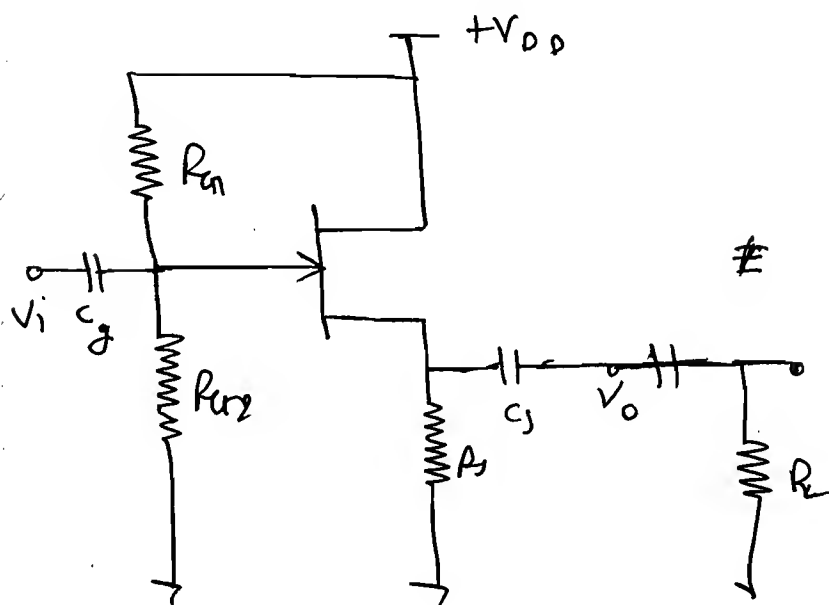
$$\therefore R_o = R_s \parallel \frac{1}{g_m}$$

$$V_o = \frac{g_m (R_d \parallel R_s)}{1 + g_m (R_d \parallel R_s)}$$

$$\text{if } R_d \gg R_s$$

$$V_o = \frac{g_m R_s}{1 + g_m R_s}$$

### ② Voltage divider:



$$\rightarrow R_i = R_{G1} \parallel R_{G2}$$

$$R_o = R_S \parallel \frac{1}{g_m}$$

$$A_v = \frac{g_m \cdot R_S}{1 + g_m \cdot R_S}$$

if  $R_L$  is connected,

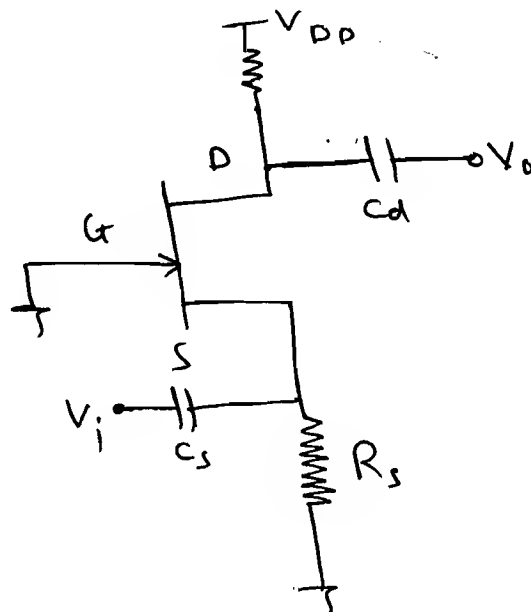
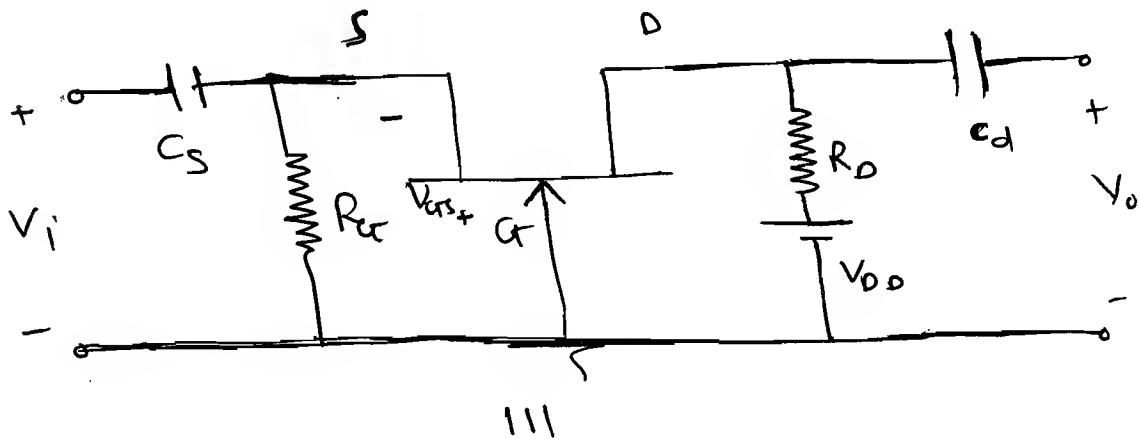
$$R_i = R_{G1} \parallel R_{G2}$$

$$R_o = R_S \parallel \frac{1}{g_m} \parallel R_L$$

$$A_v = \frac{g_m \cdot (R_S \parallel R_L)}{1 + g_m(R_S \parallel R_L)}$$

### ③ Common gate Configuration Amp.

$\Rightarrow$



$$R_i \approx R_S \parallel \frac{1}{g_m}$$

$$R_o = r_{d1} \parallel R_D$$

$$A_v = g_m (r_{d1} \parallel R_D)$$

if  $r_{d1} \gg R_D$

$$R_o \approx R_D$$

$$A_v \approx g_m R_D$$

\*

## BJT

$$C_B = 0$$

$$C_E = 180^\circ$$

$$C_C = 0$$

## FET

$$C_G = 0$$

$$C_S = 180^\circ$$

$$C_D = 0$$

### ① BJT:

	$A_I$	$A_V$
CB :	$\approx 1$	High
CE :	High	High
CC :	High	$\approx 1$

Voltage gain	Current gain
$A_{V_{CC}} \approx 1$	$A_{I_{CB}} \approx 1$
$A_{V_{CB}} > A_{V_{CE}}$	$A_{I_{CC}} > A_{I_{CE}}$
$A_{CC} < A_{V_{CE}} < A_{V_{CB}}$	$A_{I_{CB}} < A_{I_{CE}} < A_{I_{CC}}$

### ② FET:

Voltage gain

Current gain

$$C_D: A_{V_D} = \frac{g_m R_D}{1 + g_m R_S} \approx 1$$

$$C_G: A_{I_{CG}} = \frac{I_D}{I_S} = 1$$

$$\left. \begin{array}{l} C_S: A_{V_{CS}} \\ C_G: A_{V_{CG}} \end{array} \right\} A_{V_{CG}} > A_{V_{CS}}$$

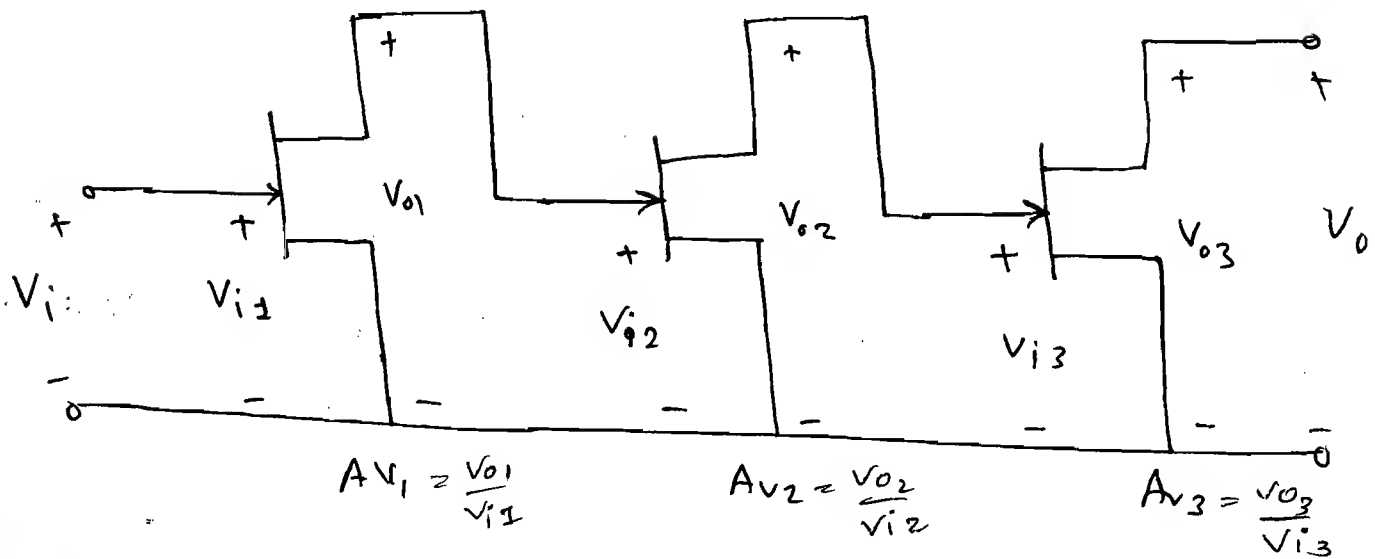
$$A_{V_{CD}} < A_{V_{CS}} < A_{V_{CG}}$$

$\Rightarrow \star$

$\Rightarrow$  So, whenever we go for the multistage amplifier we should always remember its voltage gain and current. Because voltage gain ~~is not~~ ~~current~~ ~~gain~~ decide its input and output impedance. Whenever we want to decide voltage amplifier max. power should be transfer from one stage to another stage and for that MPTT should be apply.

# ★ Multistage Amplifier:

⇒



Overall gain  $A_V = \frac{V_0}{V_i}$

$$A_V = \underbrace{\frac{V_0}{V_{03}}}_{1} \times \underbrace{\frac{V_{03}}{V_{i3}}}_{A_{V3}} \times \underbrace{\frac{V_{i3}}{V_{02}}}_{1} \times \underbrace{\frac{V_{02}}{V_{i2}}}_{A_{V2}} \times \underbrace{\frac{V_{i2}}{V_{01}}}_{1} \times \underbrace{\frac{V_{01}}{V_{i1}}}_{A_{V1}} \times \underbrace{\frac{V_{i1}}{V_i}}_{1}$$

$$A_V = A_{V3} \times A_{V2} \times A_{V1}$$

⇒ In a multistage amplifier overall voltage gain is the product of individual stage voltage gain provided that there should not be any series resistance bet<sup>n</sup> two stages but shunt resistance can be allowed.

⇒ In multistage current amplifier overall current gain is the product of individual stage current gain provided that there should



not be any Shunt resistance b/w two stages but series resistor can be allowed.

=> Multistage are divided into Four

Parts:

- ① Cascade
- ② Cascode
- ③ Denignton
- ④ Parallel.

① Cascade Connection: (for getting high voltage gain)

=> For BJT:

CB:  $\frac{Z_{in}}{\text{High}}$   $\frac{Z_o}{\text{Low}}$

CE: High High

CC: Low High.

We can connect

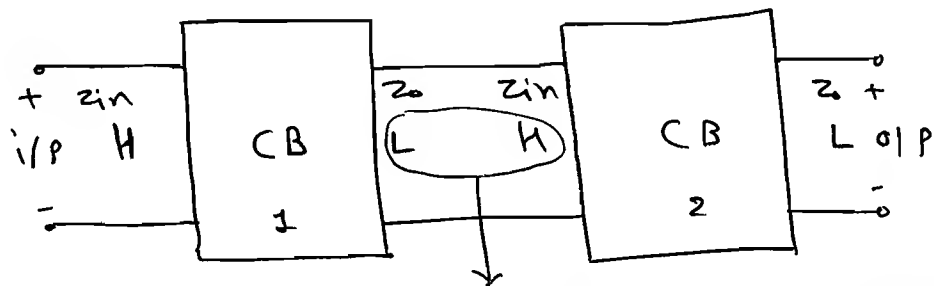
CB - CB

CE - CE

CC - CC.

Possible but all are not valid.

① CB - CB:

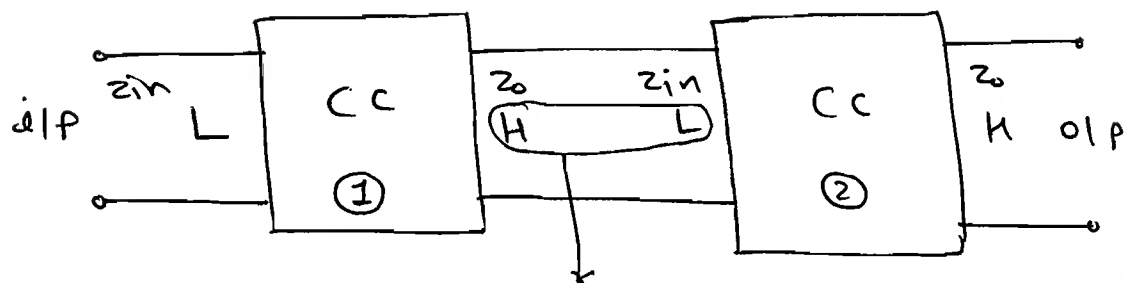


max. power not transfer from stage 1 to 2.

So, even though CB has high voltage gain it can not be used in case-cascade connection, for <sup>over</sup> high voltage gain.

② CE - CE:

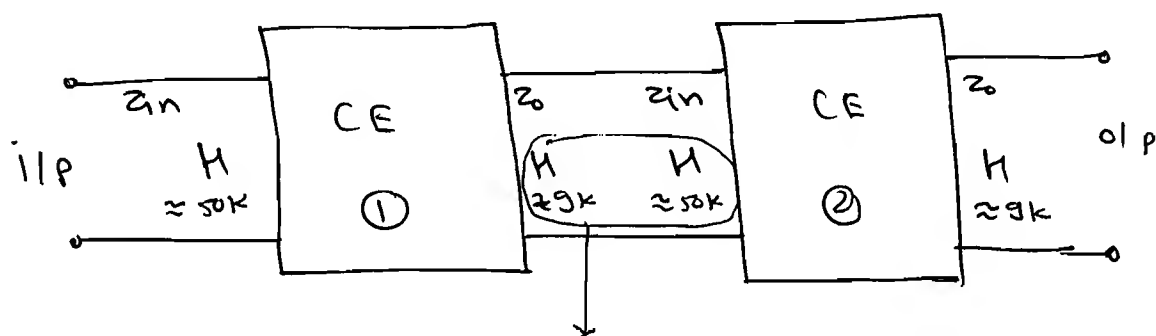
⇒



max. power will not be transfer from stage ① to ②.

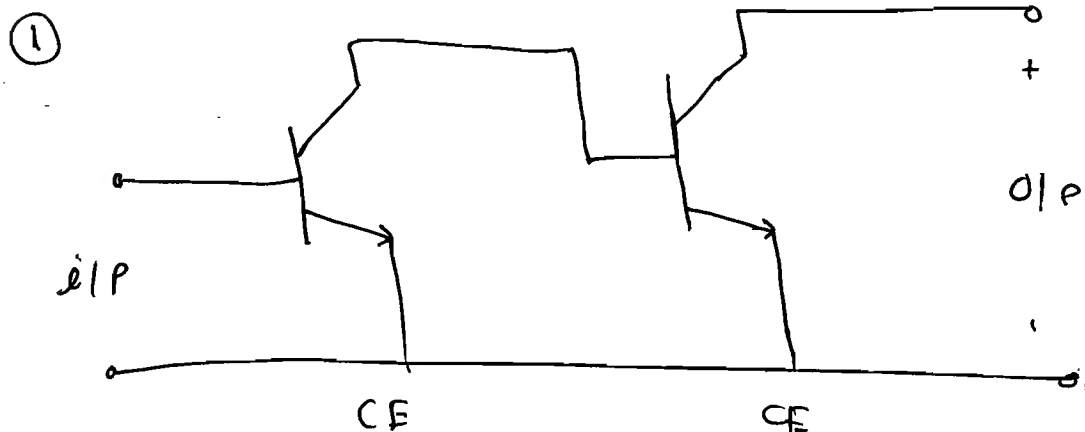
so, CC has voltage gain almost 1 and it also not used in voltage amp.

### ③ CE - CE:



due to this we can get max. power transfer from stage - ① to ②.

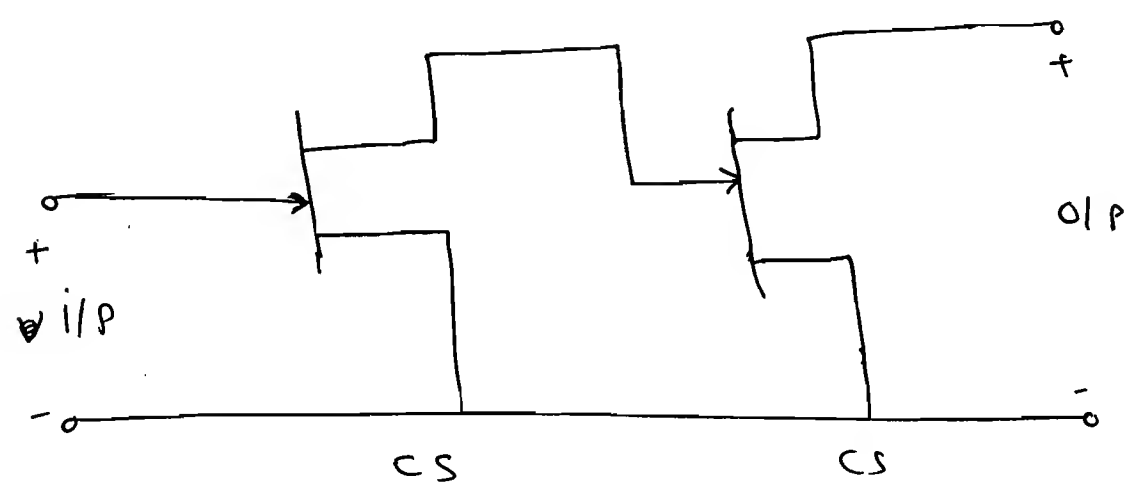
⇒ Therefore, In most of the practical application we use CE - CE cascade amplifier.



② For FET:

⇒ Same concept is applied into FET.

① So, only one possible way is CS-CS  
Cascode connection for voltage amplifier.



② Case-Cade Connection: (for High Bandwidth & i/p impedence) getting.

⇒ ① For BJT:

CE      CB      CC

⇒ As there are three configuration (CE, CB, CC), there are six possible way to make case-cade connection.

① CE - CB      Valid  
H (H) ✓ (H) L

④ CB - CE      X not valid  
H (L) x (H) H

② CE - CC      Invalid  
H (H) x (L) H

⑤ CC - CE      Valid  
L (H) ✓ (H) H

③ CB - CC      Valid  
H (L) ✓ (L) H

⑥ CC - CB      Valid  
L (H) ✓ (H) H

$\Rightarrow$  Among six possibility, four are valid for wide band structure and case code connection.

From that,

We can say that CB-CC & CC-CB are same because it is a just matter of order. i.e. first CB (or) CC no matter, it work same.

$\Rightarrow$  But, in CB-CC, ~~input~~  $z_{in} = \text{high}$ ,  $z_o = \text{high}$  whereas

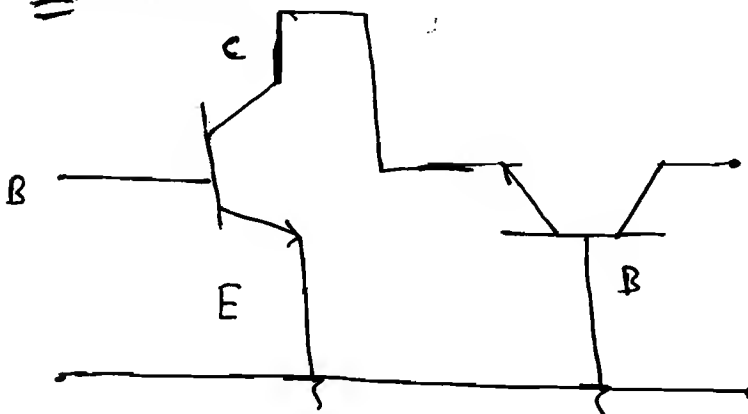
in CC-CB  
 $z_{in} = \text{Low}$ ,  $z_o = \text{high}$ . so it provide

better gain compare to CB-CC.

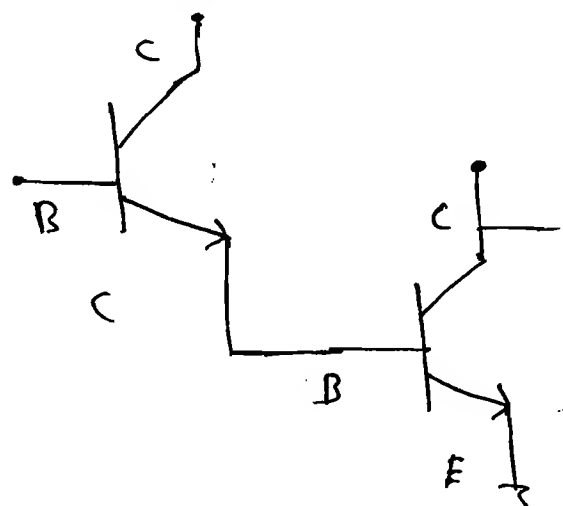
so, wide band structures (or) case code connections are.

① CE-CB ② CC-CE ③ CC-CB.

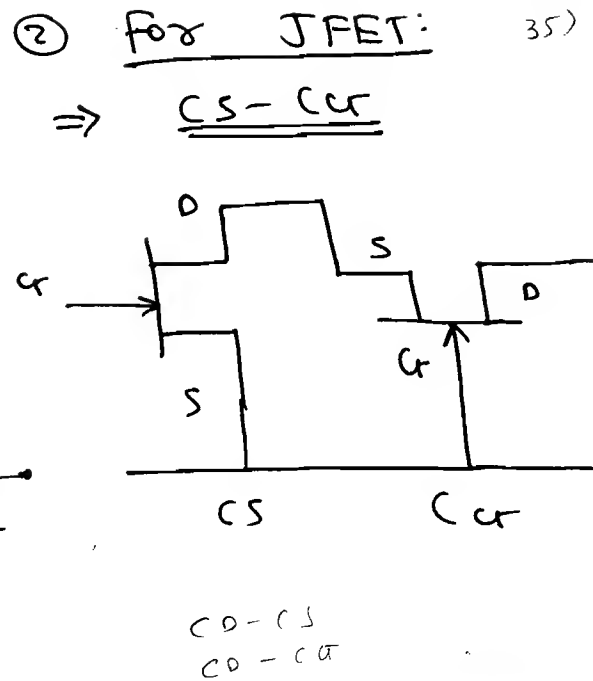
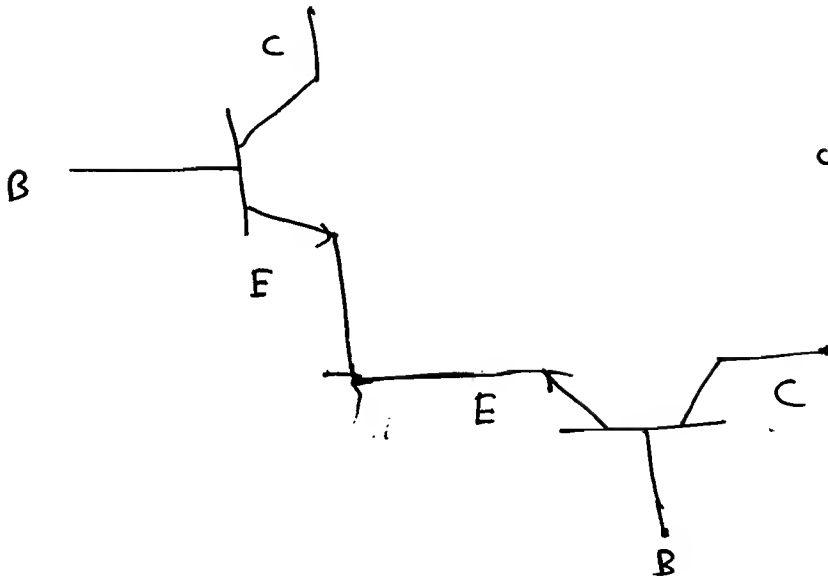
① CE-CB:



② CC-CE



③ CC-CB:



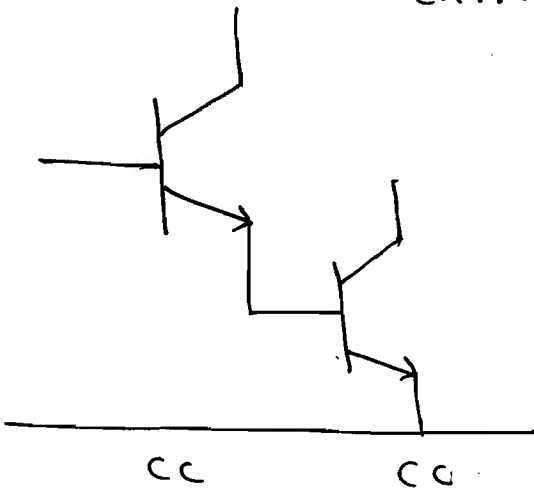
③ Darlington

Connection: (for getting high current gain)

① For BJT

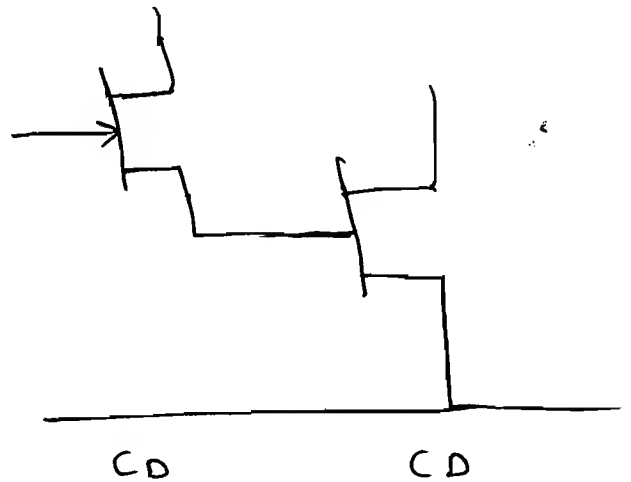
$C_E - C_C$

For large current gain



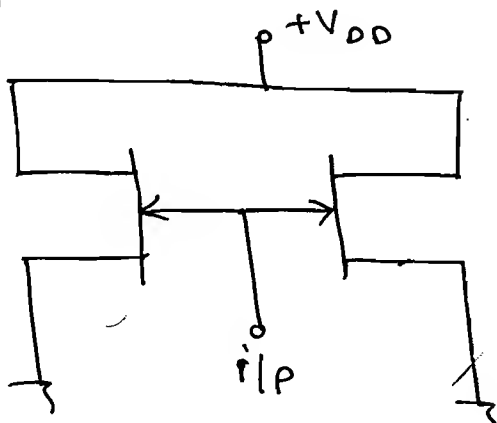
② For FET

$C_D - C_D$

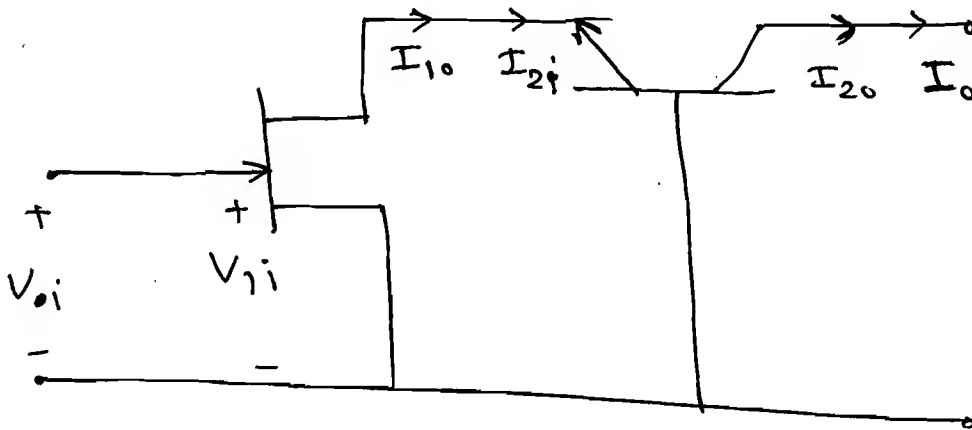


④ Pushout: (to increasing current rating)

$\Rightarrow$  FET



Q For the Ckt Shown in the fig.  
 FET has trans Conductance of  $5 \text{ mA/V}$  and  
 BJT has a ~~CB~~ CB Current gain  $0.8$ .  
 Calculate overall trans conductance of the  
 Composite amp.



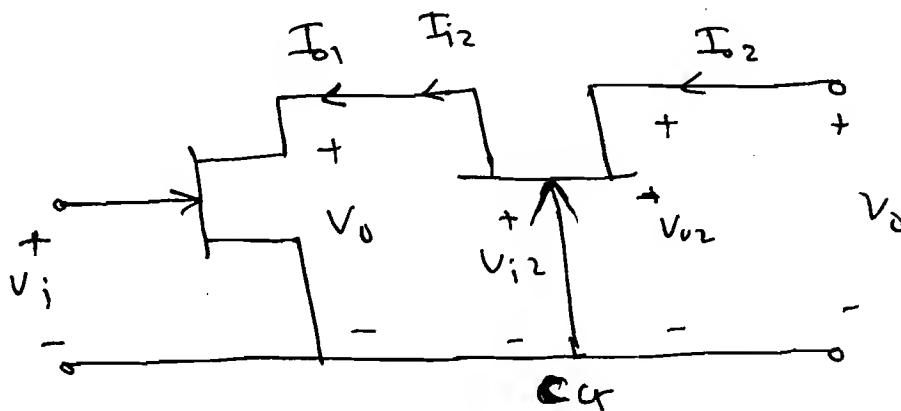
Sol<sup>n</sup>:

$$\therefore g_m = \frac{I_o}{V_i} = \underbrace{\frac{I_o}{I_{2o}}}_{1} \times \underbrace{\frac{I_{2o}}{I_{2i}}}_{0.8} \times \underbrace{\frac{I_{2i}}{I_{10}}}_{1} \times \underbrace{\frac{I_{10}}{V_{ii}}}_{5 \text{ mA/V}} \times \underbrace{\frac{V_{ii}}{V_{oi}}}_{1}$$

$$\therefore g_m = 0.8 \times 5$$

$$g_m = 4 \text{ mA/V.}$$

Q-2



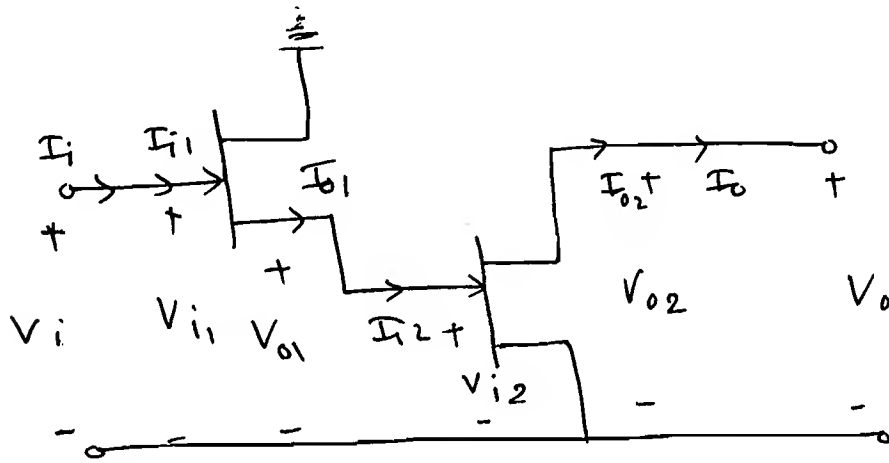
$\Rightarrow$  For the Ckt shown in the fig. transistor  
 $M_1$  &  $M_2$  has trans Conductances of  $g_{m1}$  &  $g_{m2}$ .  
 Calculate the overall trans conductance of the  
 Composite amplifier.

$\Rightarrow$  overall  $g_m = \left( \frac{I_{o1}}{I_{o2}} \right) \times \left( \frac{I_{o2}}{I_{i2}} \right) \times \left( \frac{I_{i2}}{I_{o1}} \right) \times \left( \frac{I_{o1}}{V_{i1}} \right) \times \left( \frac{V_{i1}}{V_i} \right)$

$\downarrow$   $\downarrow$   $\downarrow$   $\downarrow$   $\downarrow$   
 $1$   $1$   $1$   $g_{m1}$   $1$

$\boxed{g_m = g_{m1}}$

**Q-3** For the CKT shown in the figure transistor  $M_1$  &  $M_2$  has transconductance of  $g_{m1}$  &  $g_{m2}$ . Calculate overall transconductance.



$\therefore$  Soln:  $g_m = \frac{I_o}{V_i} = \left( \frac{I_{o2}}{I_{o1}} \right) \times \left( \frac{I_{o2}}{V_{i2}} \right) \times \left( \frac{V_{i2}}{V_{o1}} \right) \times \left( \frac{V_{o1}}{V_{i1}} \right) \times \left( \frac{V_{i1}}{V_i} \right)$

$\downarrow$   $\downarrow$   $\downarrow$   $\downarrow$   $\downarrow$   
 $1$   $g_{m2}$   $1$   $1$   $1$

$\therefore \boxed{g_m = g_{m2}}$

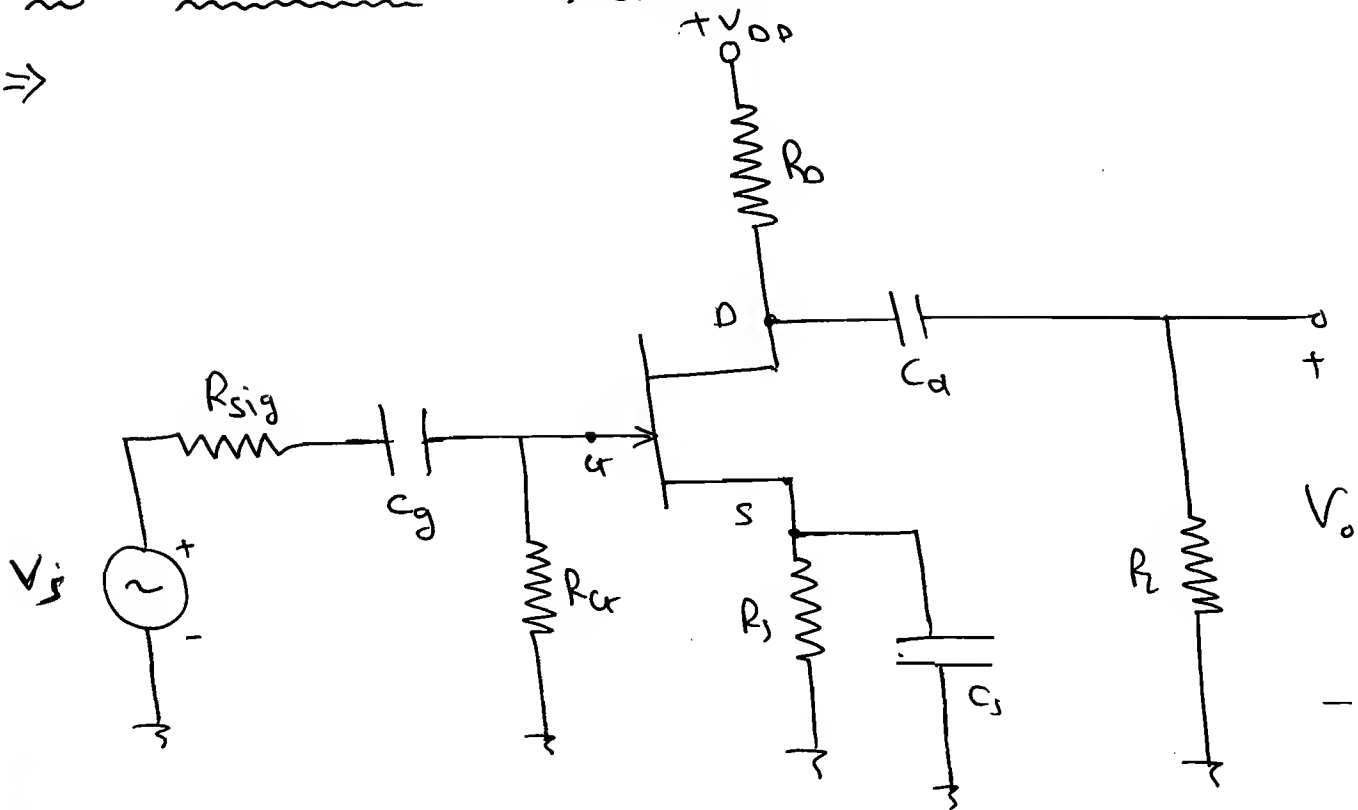


Frequency

Response

Analysis:

⇒



⇒  $C_g, C_d$  &  $C_S$ : Coupling and bypass cap.

$$X_c = \frac{1}{\omega C} = \frac{1}{2\pi f C}$$

DC:  $f = 0 \Rightarrow X_c = \infty$  so, o.c for D.C.

\*  $C_g$ :

⇒ It blocks the d.c. signals enters from source to input stage of the amplifier.

⇒ It blocks the d.c. signals enters from the 'i/p stage of the amplifier to the source.

⇒ It isolates the input stage of the amp from the source d.c. point of view i.e. act like a open ckt for d.c. signals.

⇒ It couples the signals from source to



input of the amplifier. i.e. it acts like a short circuit for a.c. signals.  
 $\Rightarrow$  It avoids the loading effect due to signal resistor

\*  $C_d$ : (4F)

$\Rightarrow$  It blocks the d.c. signals from the o/p stage of amplifier to the load.

$\Rightarrow$  It isolates the o/p stage of amp. from the load d.c. point of view. i.e. it acts like an open circuit for the d.c.

$\Rightarrow$  It couples the a.c. signals from the o/p stage of amplifier to the load for a.c. signals.

\*  $C_s$ :

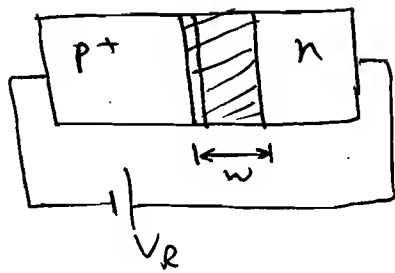
$\Rightarrow$  It avoids the -ve feedback due to source resistor  $R_s$ .

$\Rightarrow$  It bypasses A.c. signals through it.

$C_g, C_d, C_s$  : (4F) (4.7 4F, 10 4F)

$\rightarrow$  Always prefer short circuit for A.c. signals.

① R.B.



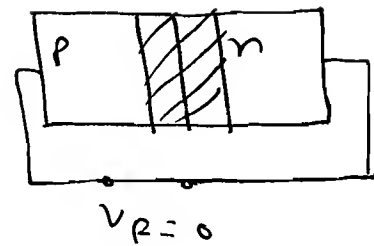
$$C = \frac{\epsilon A}{w}$$

Transition Capacitance

$$C_T = \frac{C_{T0}}{\left(1 + \frac{V_R}{V_0}\right)^{1/2}}$$

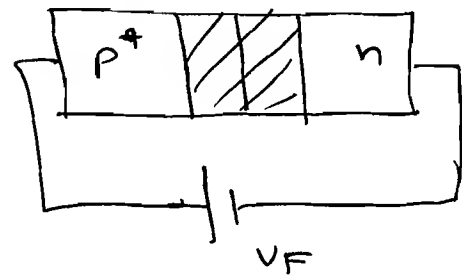
$1/2$  for linear

② O.C.

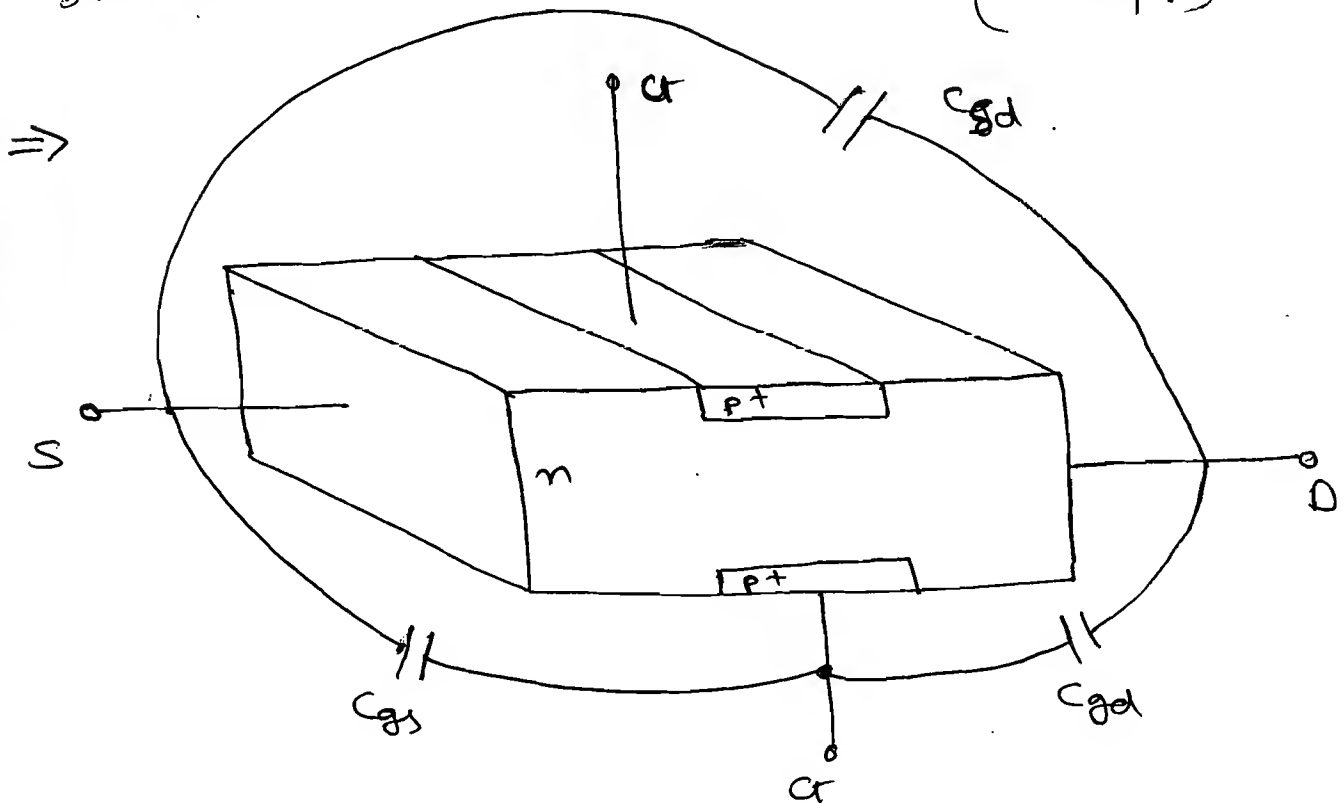


$$\epsilon_0 = \epsilon A / w$$

③ F.B. (Diffusion Cap.)



$$C_j = \frac{C_{j0}}{\left(1 + V_R / V\right)^{1/2}}$$



$\therefore C_{gs}, C_{gd} \& C_{as}$ : Junction Capacitors

$\Rightarrow$  Always prefer open circuit for

$X_C = \frac{1}{\omega C} = \frac{1}{2\pi f C}$  all A.C. signals.

$C_{gs}, C_{gd}$  (1 to 10 pF)  
 $C_{sd}$  (1 to 1 pF)

### \* Low Freq.

$\Rightarrow$  Coupling Capacitor & Bypass Capacitor : O.C.  
 $\Rightarrow$  Junction Capacitors : O.C.

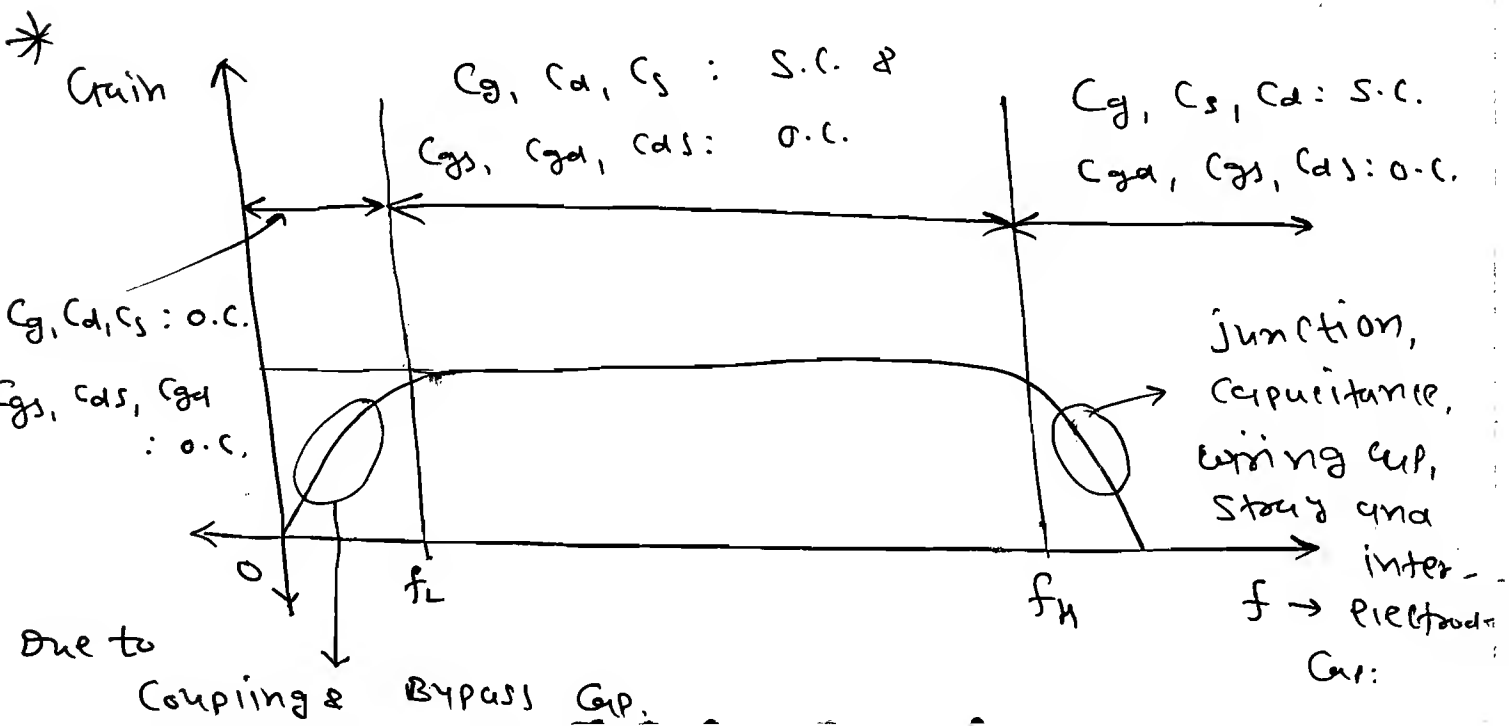
### \* Medium Freq.

$\Rightarrow$  Coupling Capacitor & Bypass Capacitor : S.C.  
 $\Rightarrow$  Junction Capacitors : O.C.

### \* High Freq.

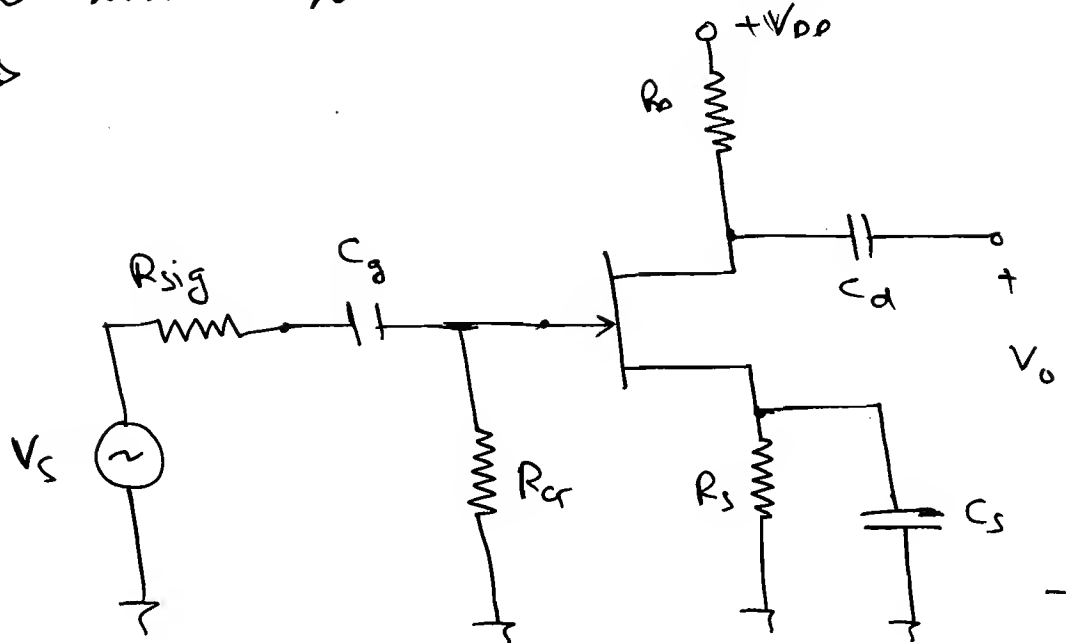
$\Rightarrow$  Coupling & Bypass Capacitors : S.C.  
 $\Rightarrow$  ~~Coupling~~ Junction Capacitors : S.C.

	Coupling & Bypass Capacitor	Junction Capacitors.
LF	O.C.	O.C.
MF	S.C.	O.C.
HF	S.C.	S.C.

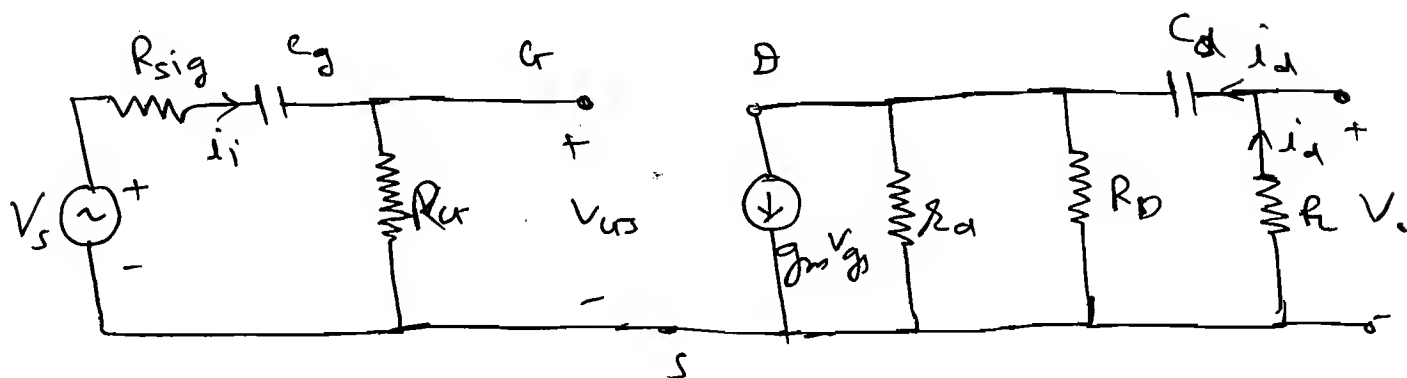


# ☆ Low Frequency Analysis:

⇒



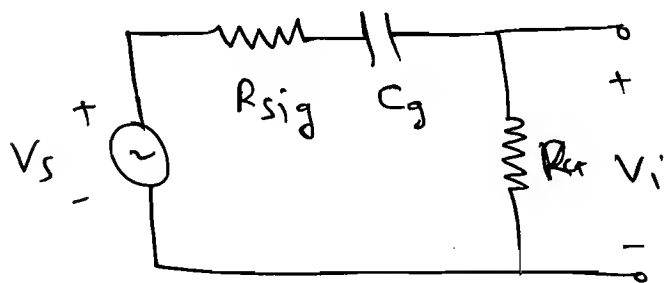
⇒ Small signal eq<sup>n</sup> (kt.)



① Input side,

$$V_s = V_{sig} + V_{cg} + V_i$$

$$\Rightarrow V_i = V_s - V_{sig} - V_{cg}$$



$$H(j\omega) = \frac{V_i}{V_s} = \frac{R_G}{R_G + R_{sig} + j\omega C_g}$$

$$\therefore H(j\omega) = \frac{R_G}{R_G + R_{sig} + j\omega C_g (R_G + R_{sig})}$$

$$\Rightarrow H(j\omega) = \frac{A_0}{1 + j \frac{1}{2\pi f C_g (R_{eq} + R_{sig})}}$$

$$\therefore H(j\omega) = \frac{A_0}{1 + j \frac{f_L}{f}}$$

where,

$$f_L = \frac{1}{2\pi C_g (R_{eq} + R_{sig})}$$

$$|H(j\omega)| = \frac{1}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}}$$

$$\text{as } C_d < C_g < C_s$$

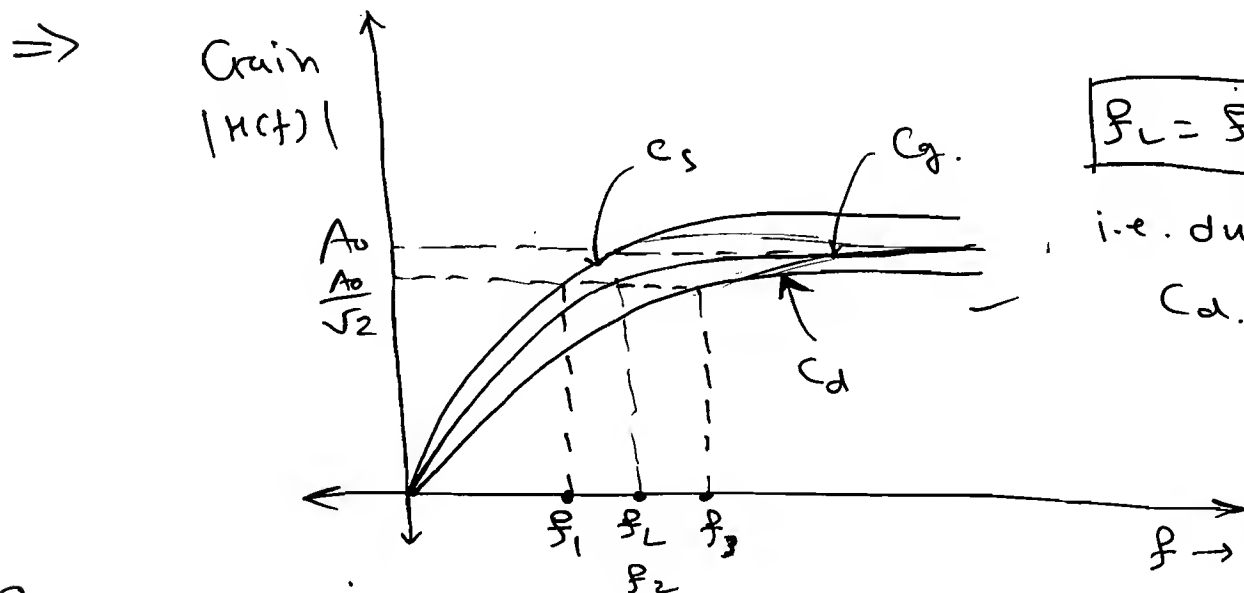
$$\Rightarrow f_d > f_g > f_s$$

$$\checkmark \text{ so } \boxed{f_L = f_d} = f_{L3}$$

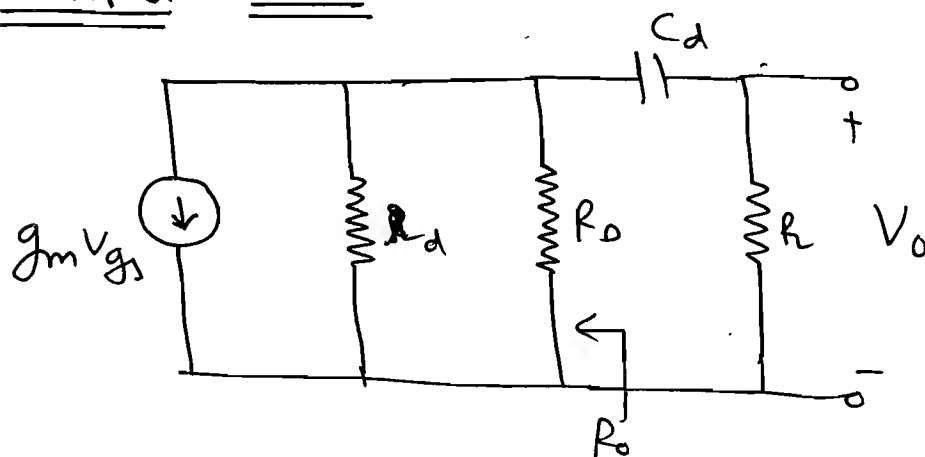
$$\Rightarrow f = 0 \Rightarrow H(j\omega) = 0$$

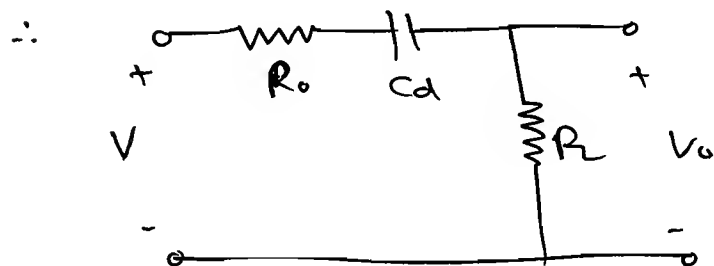
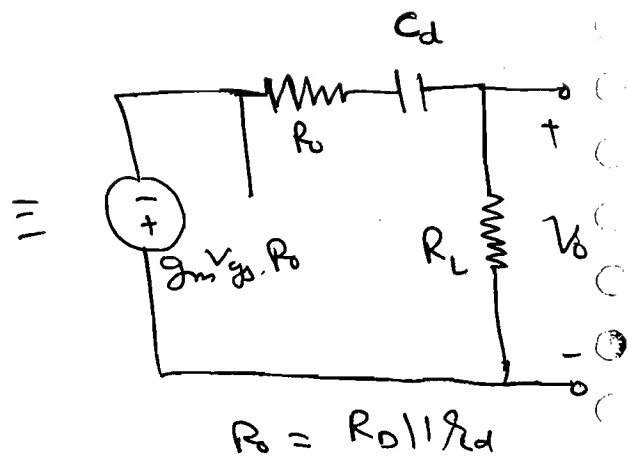
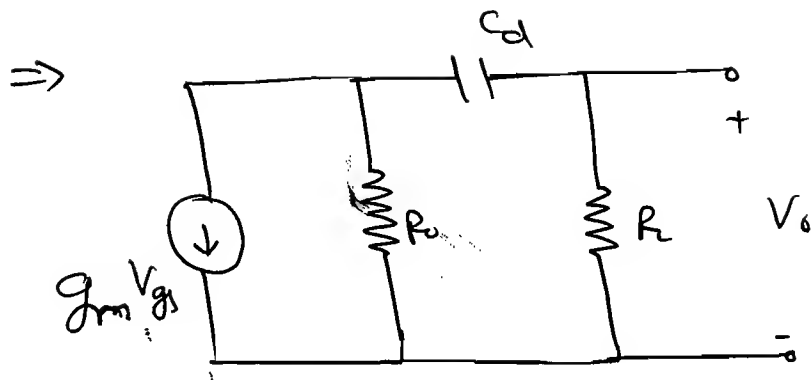
$$f = f_L \Rightarrow H(j\omega) = A_0 / \sqrt{2}$$

$$f = f_H = \infty \Rightarrow |H(j\omega)| = A_0$$



② Output side:





$\Rightarrow H(f) = \frac{R_L}{R_o + R_L + \frac{j}{j f 2 \pi C_d}}$

$H(f) = \frac{\frac{R_L}{R_o + R_L}}{1 + \frac{1}{j f 2 \pi C_d (R_o + R_L)}}$

$\therefore H(f) = \frac{A_L}{1 + j \left( \frac{f_L}{f} \right)^2}$

$\therefore |H(f)| = \frac{A_L}{\sqrt{1 + \left( \frac{f_L}{f} \right)^2}}$

$$f_L = \frac{1}{2 \pi C_d (R_o + R_L)}$$

if  $C_s$  is present, then

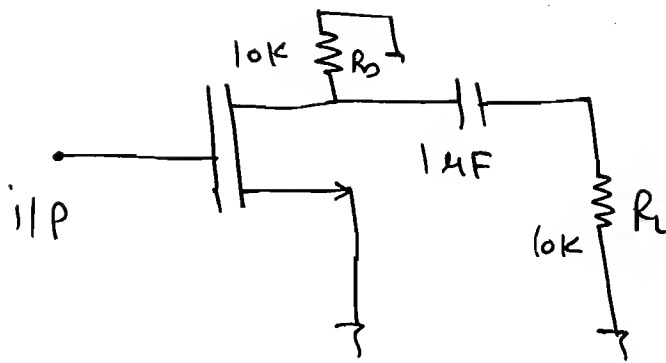
turnover

$\therefore$

$$f_L = \frac{1}{2 \pi C_s R_{eq}}$$

$R_{eq} = R_S || \frac{1}{g_m}$

Q.13 ECE



find  $f_L$ ?

Sol<sup>n</sup>:

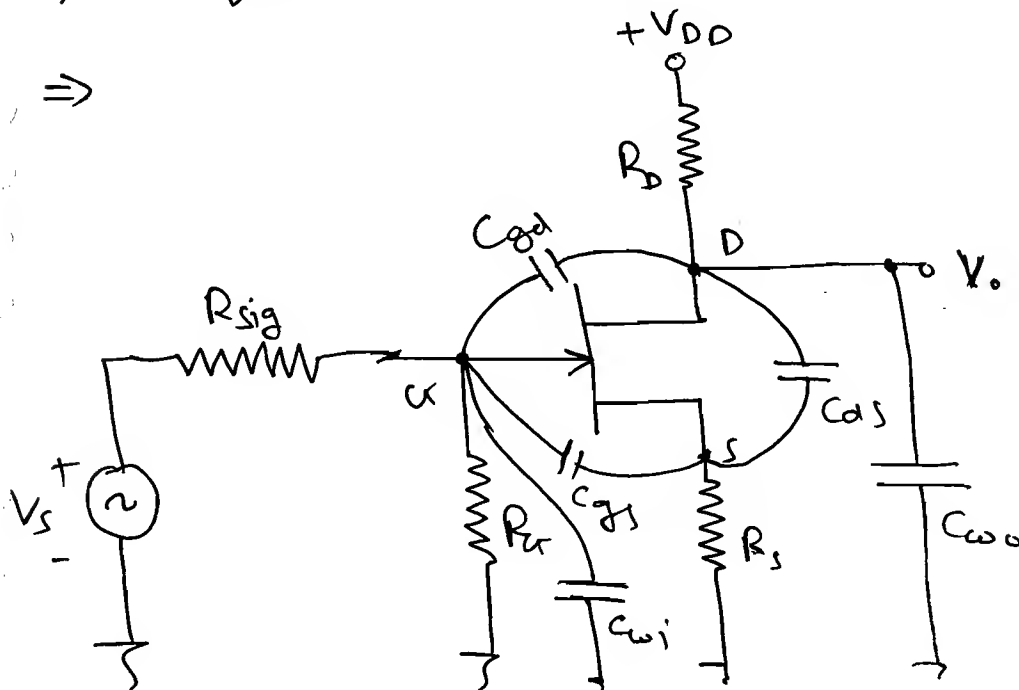
$$f_L = \frac{1}{2\pi C_d (R_D + R_L)} = \frac{1}{2\pi \times 10^{-6} \times 20 \times 10^3}$$

$$\therefore f_L = 7.96 \text{ kHz}$$

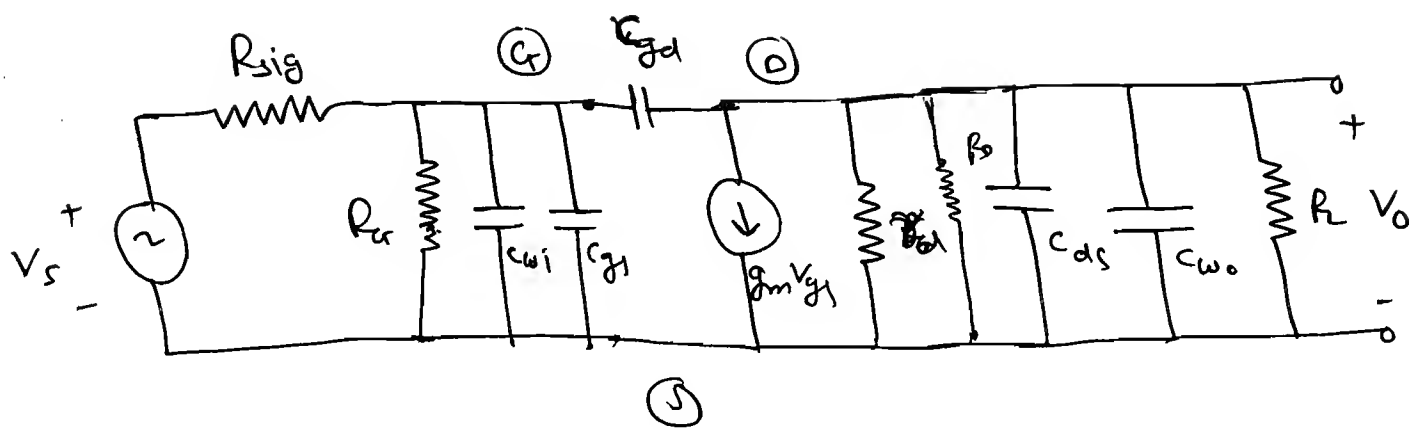
### ☆ High Frequency Analysis:

⇒ At Low freq. amplifier behaves like a high pass filter due to coupling and bypass capacitor. Therefore gain falls at low freqs. due to coupling and bypass cap.

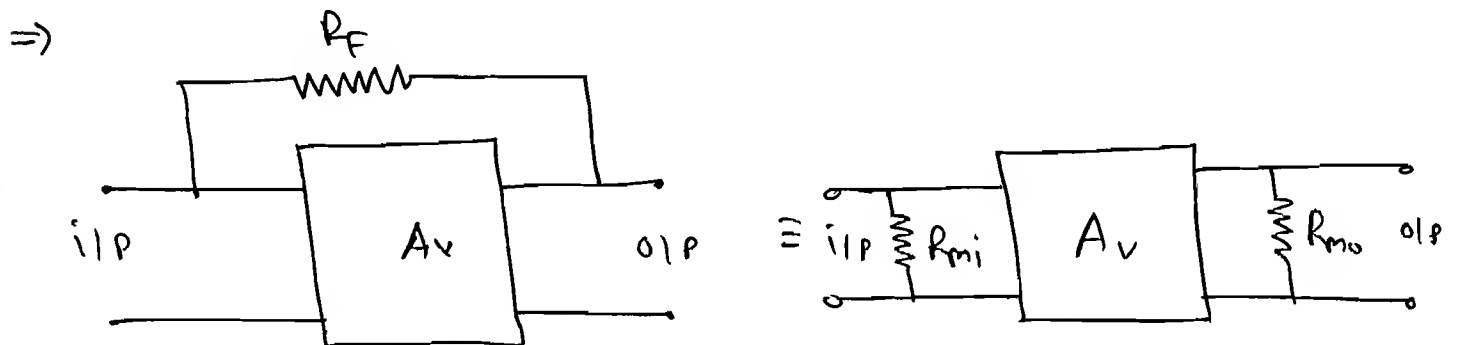
⇒



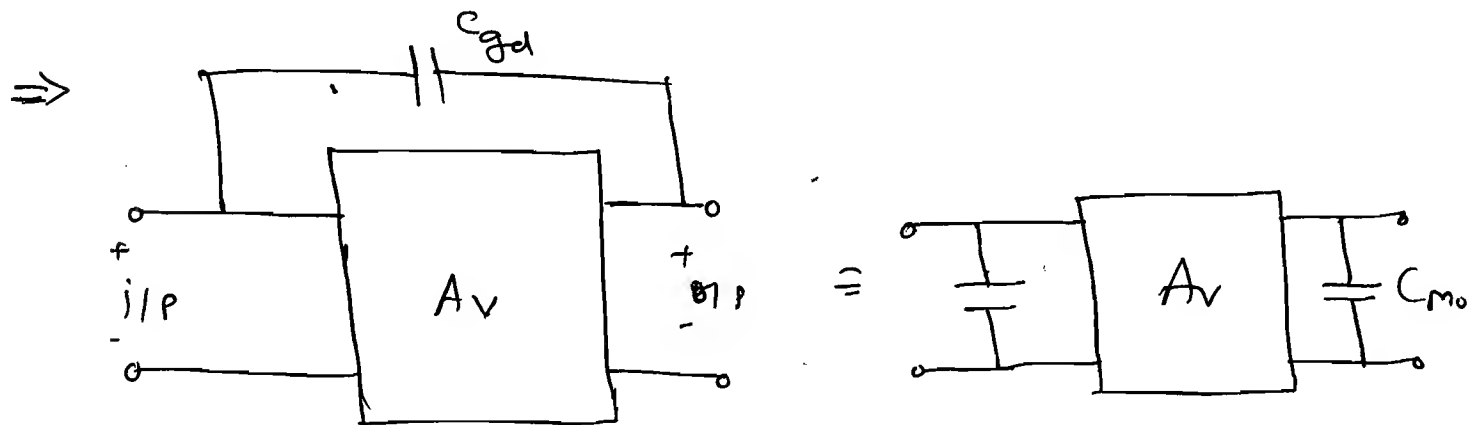
⇒ Small Signal eq<sup>n</sup> CKT:



\* Miller's Theorem:



$$R_{mi} = \frac{R_F}{1 - A_v}, \quad R_{mo} = \frac{R_F}{1 - \frac{1}{A_v}} \approx R_F \text{ for large Voltage gain.}$$

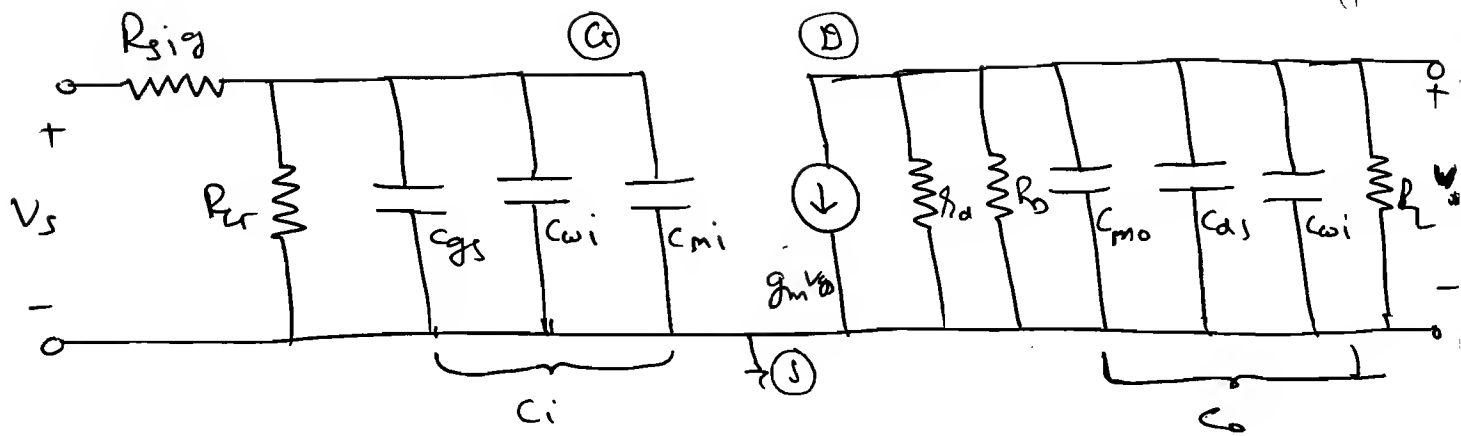


$$\Rightarrow C_{mi} = C_{gd} (1 - A_v).$$

$$C_{mo} = C_{gd} \left( 1 - \frac{1}{A_v} \right) \approx C_{gd}.$$

↑  
for large value of  $A_v$

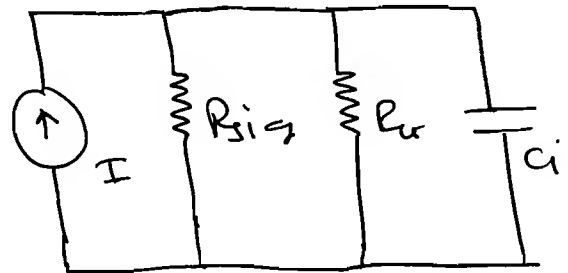




① Input side:

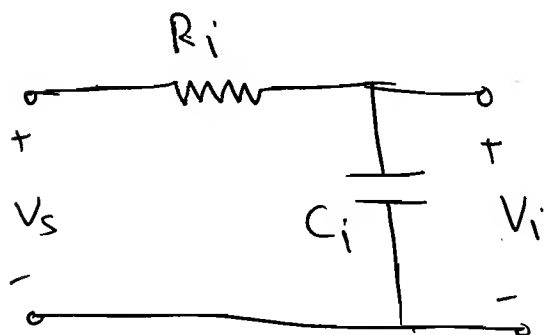


II

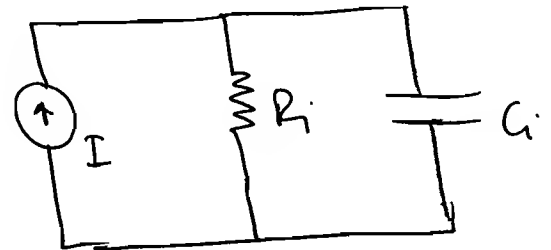


$$C_i = C_{gs} + C_{wi} + C_{mi}$$

III



II



$$R_i = R_{sig} || R_{cr}$$

$$\Rightarrow H(j\omega) = \frac{\frac{1}{j\omega C_i}}{R_i + \frac{1}{j\omega C_i}}$$

$$H(j\omega) = \frac{1}{1 + j\omega C_i R_i}$$

$$\therefore H(f) = \frac{1}{1 + j f 2\pi C_i R_i}$$

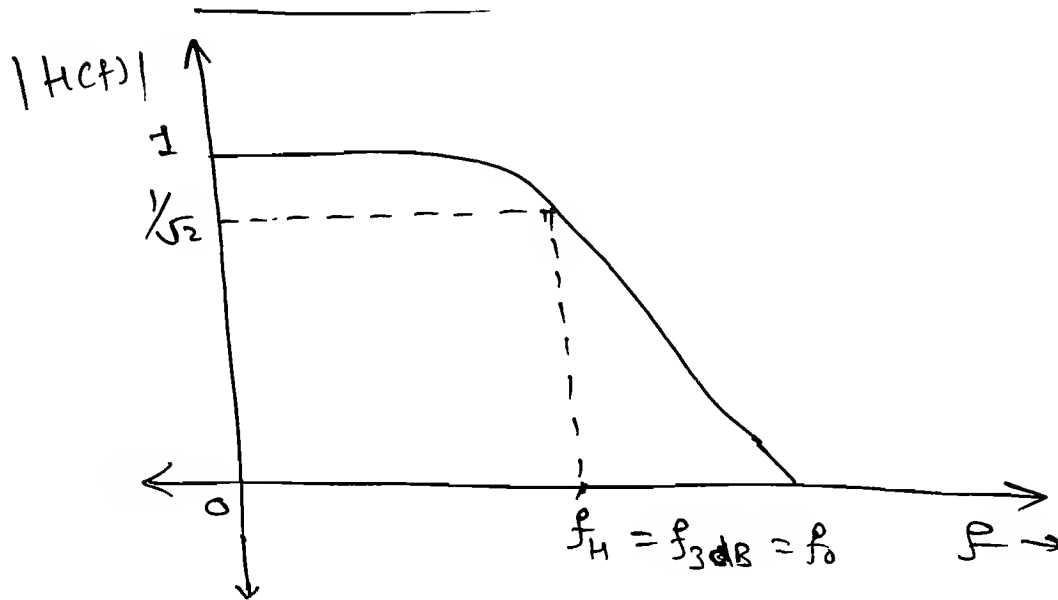
$$H(f) = \frac{1}{1 + j \frac{f}{f_H}} \Rightarrow |H(f)| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}}$$

$$\therefore f_H = \frac{1}{2\pi C_i R_i}$$

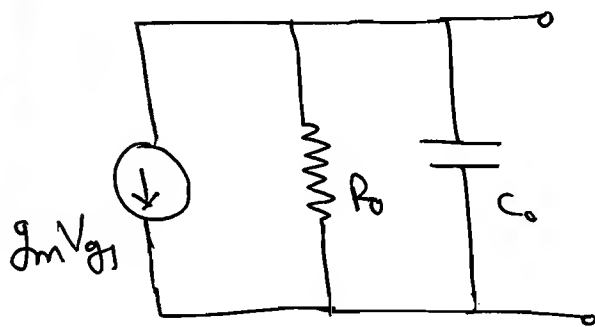
$$\Rightarrow \text{for } f=0 \Rightarrow |H(f)| = 1.$$

$$\text{for } f=f_H \Rightarrow |H(f)| = 1/\sqrt{2}.$$

$$\text{for } f=\infty \Rightarrow |H(f)| = 0.$$

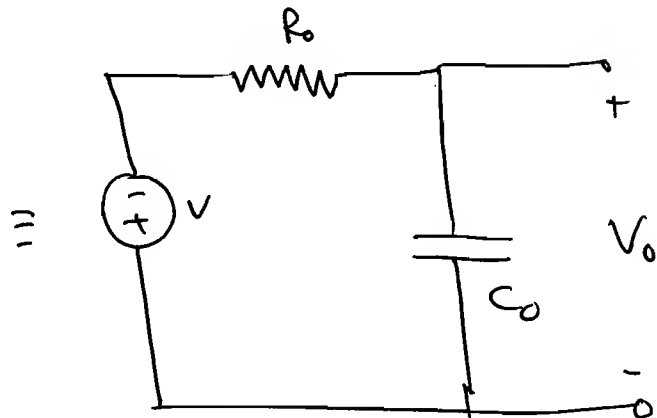


② O/P side:



$$H(f) = \frac{1}{1 + jf 2\pi C_0 R_0}$$

$$h(f) = \frac{1}{1 + j f / f_H}$$



$$R_0 = R_L \parallel R_d \parallel R_0$$

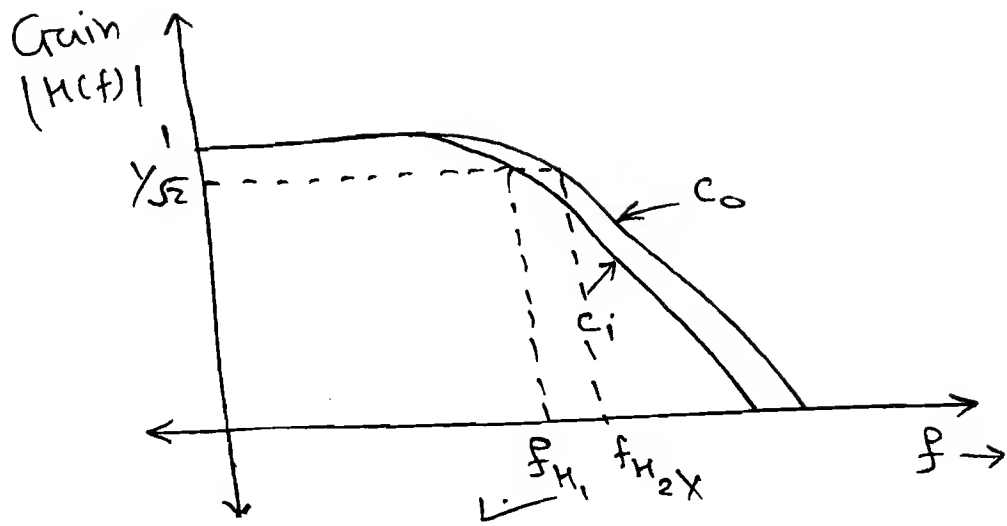
$$R_0 = R_L \parallel R_0 \quad (\because g_m \gg R_0)$$

$$C_0 = C_{m0} + C_{w0} + C_{cs}$$

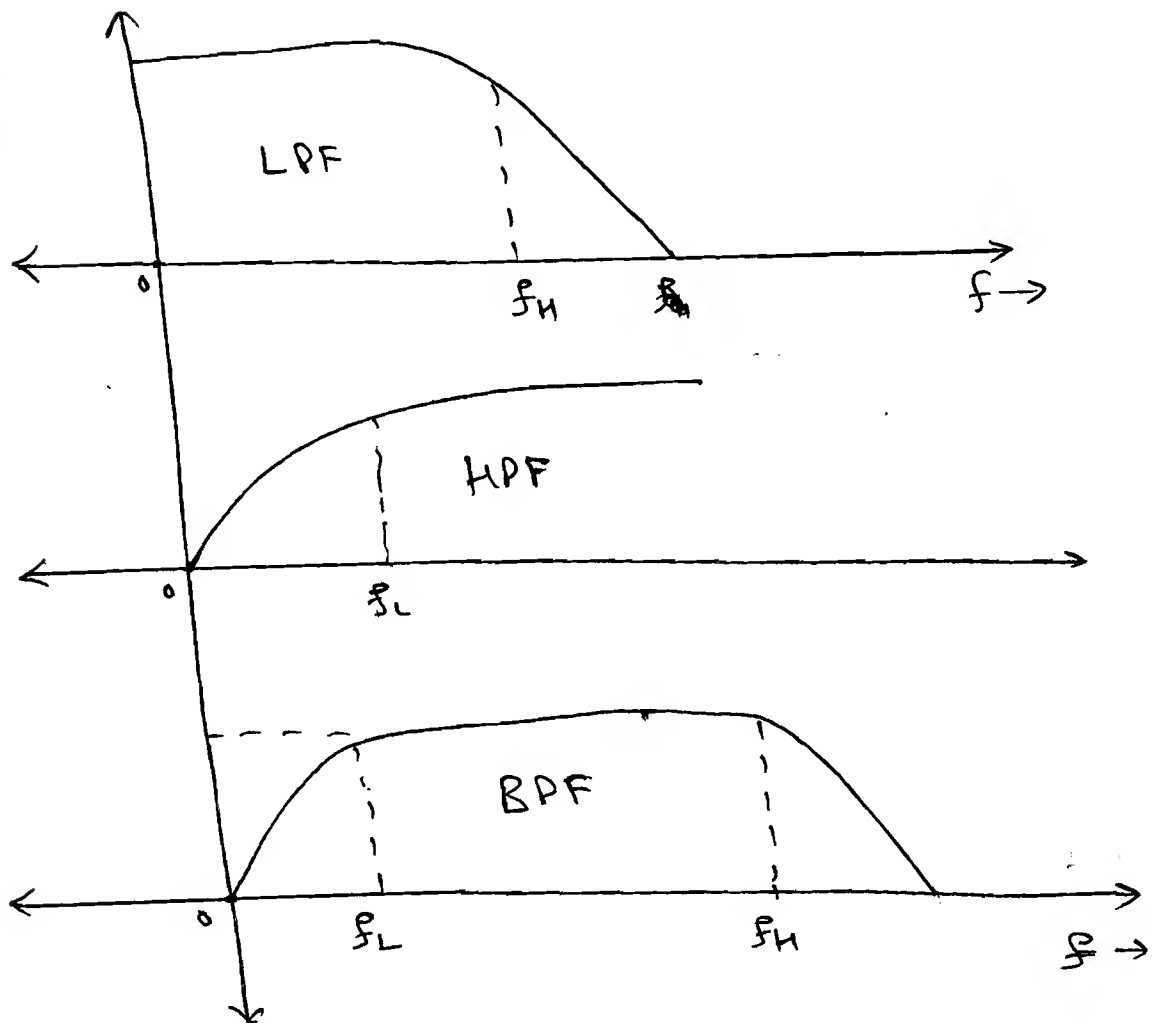
$$\therefore |H(f)| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}}$$

$$f_H = \frac{1}{2\pi R_0 C_0}$$

⇒



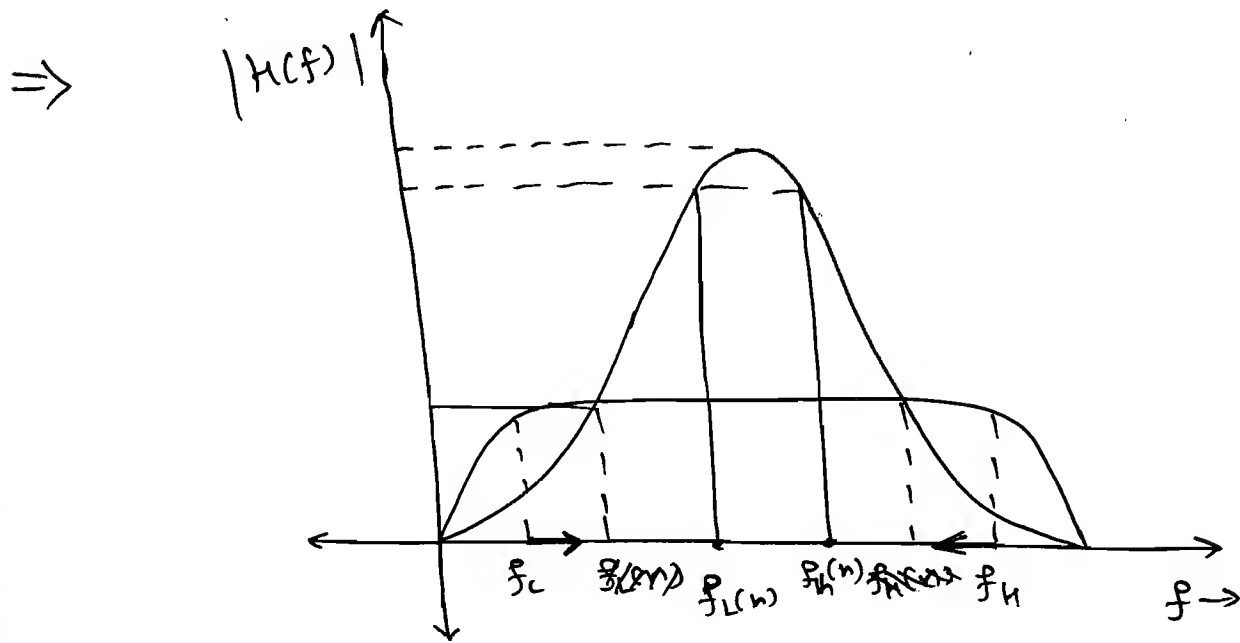
⇒



⇒ At high freq. Amp. behaves like a LPF due to junction, wiring, stray and inter-electrode capacitance. Therefore, gain falls at high frequency due to junction, wiring, stray and interelectrode capacitance.

$\Rightarrow$  Amplifier is behaving like a hpf at Low freq. and is behaving like a LPF at high freq. Therefore, amplifier is

a BPF.



$$BW = f_H - f_L$$

$$f_L(n) = \frac{f_L}{\sqrt{2^{\frac{1}{n}} - 1}}$$

$$f_H(n) = f_H \sqrt{2^{\frac{1}{n}} - 1}$$

$$BW(n) = f_H(n) - f_L(n)$$

$$BW(n) = B.W. \sqrt{2^{\frac{1}{n}} - 1}$$

\* Drawback of JFET:

$\Rightarrow$  more gate leakage current.

i.e. more  $I_{GSS}$

$\Rightarrow$  large size.

$\Rightarrow V_{DS}$  &  $V_{GS}$  have different polarities.

n-JFET

$V_{DS}$ : +ve

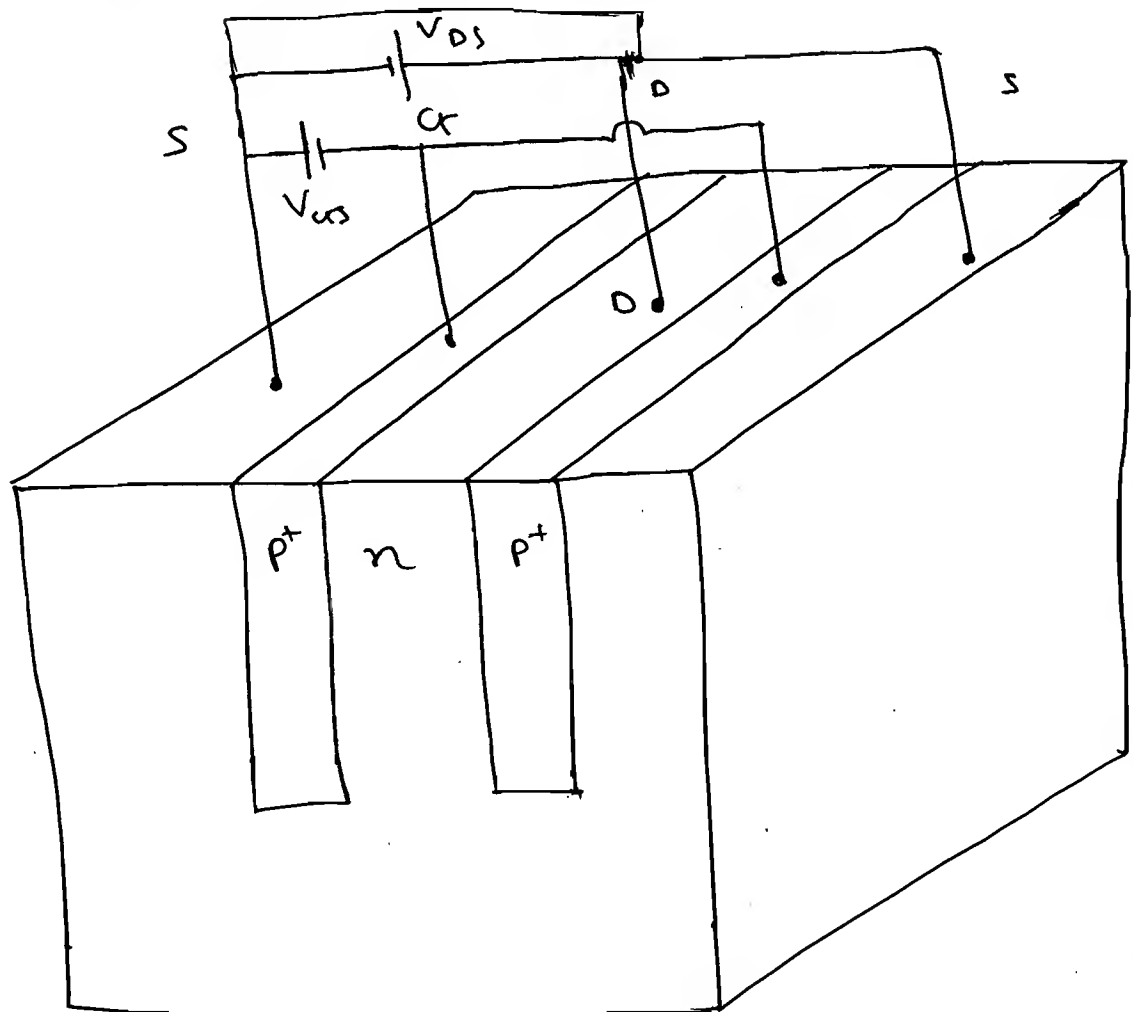
$V_{GS}$ : -ve

p-JFET

$V_{DS}$  = -ve

$V_{GS}$  = +ve.

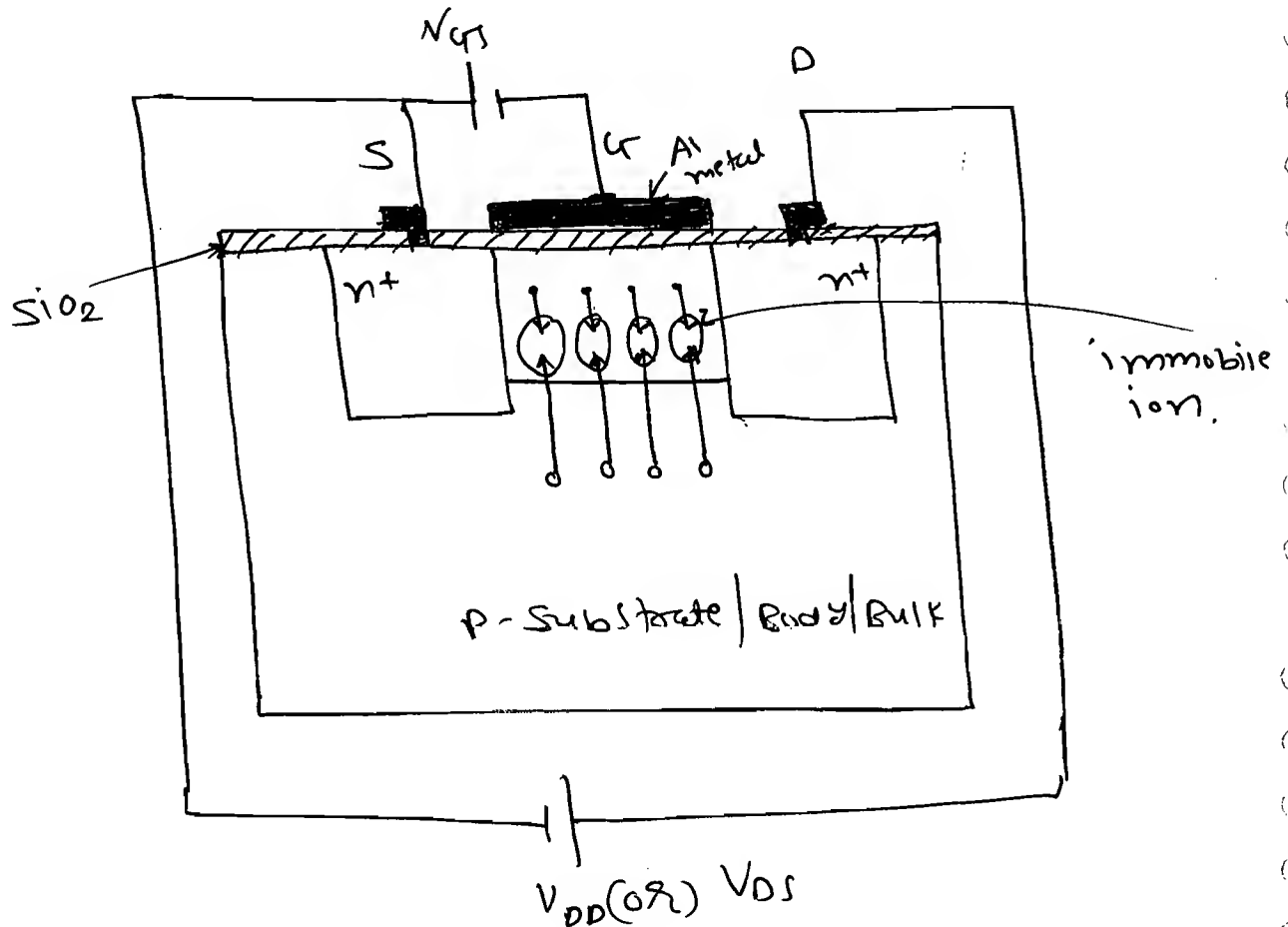
$\Rightarrow$  Now, a days following const<sup>n</sup> of  $\otimes$  FET is used.



# ★ Depletion MosFET:

① n-channel Depletion MosFET: (n-DMOSFET)

⇒



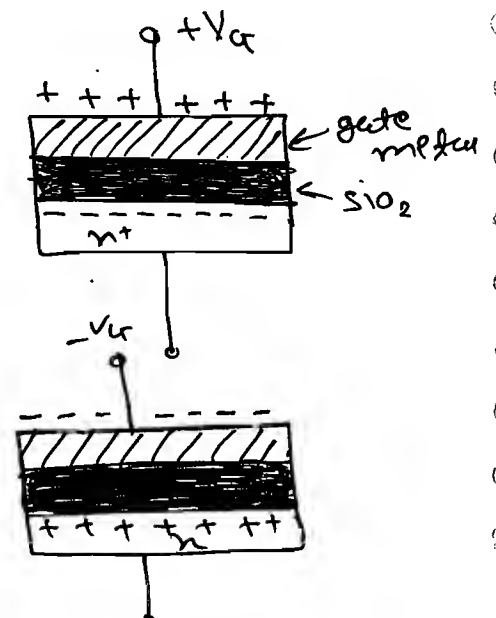
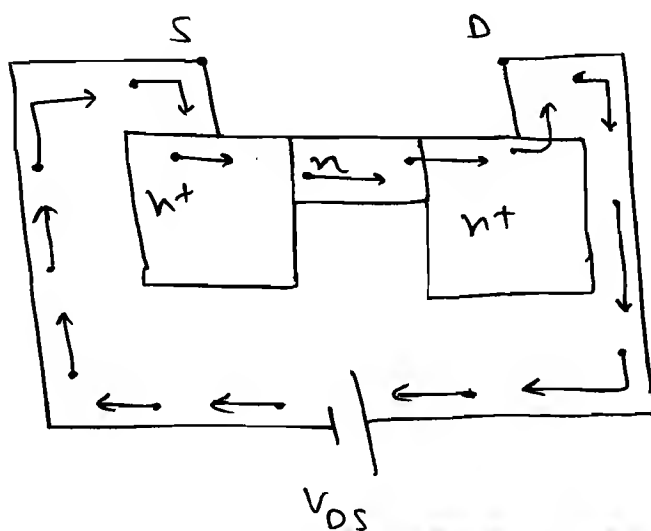
⇒

$$R_{iBJT} < R_{iJFET}$$

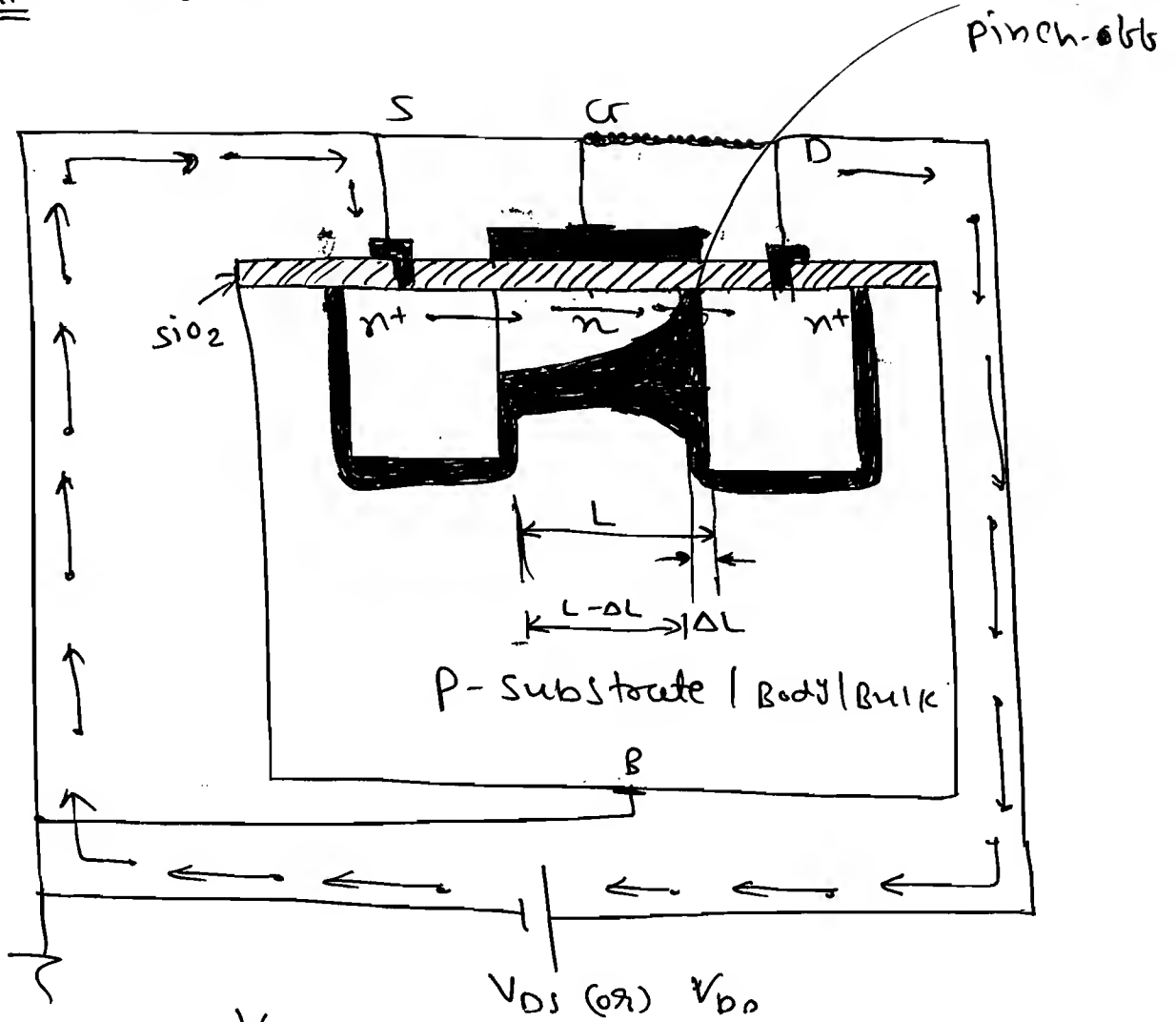
$$R_{iJFET} < R_{iMOSFET}$$

$$\therefore R_{iBJT} < R_{iJFET} < R_{iMOSFET}$$

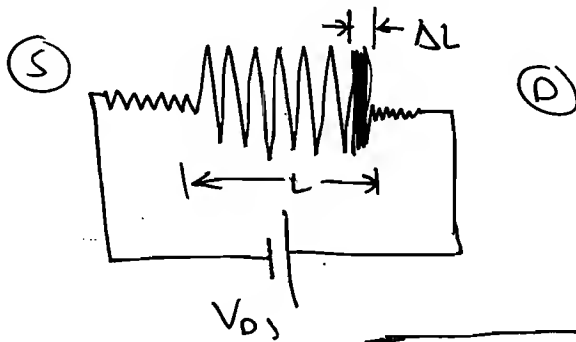
⇒



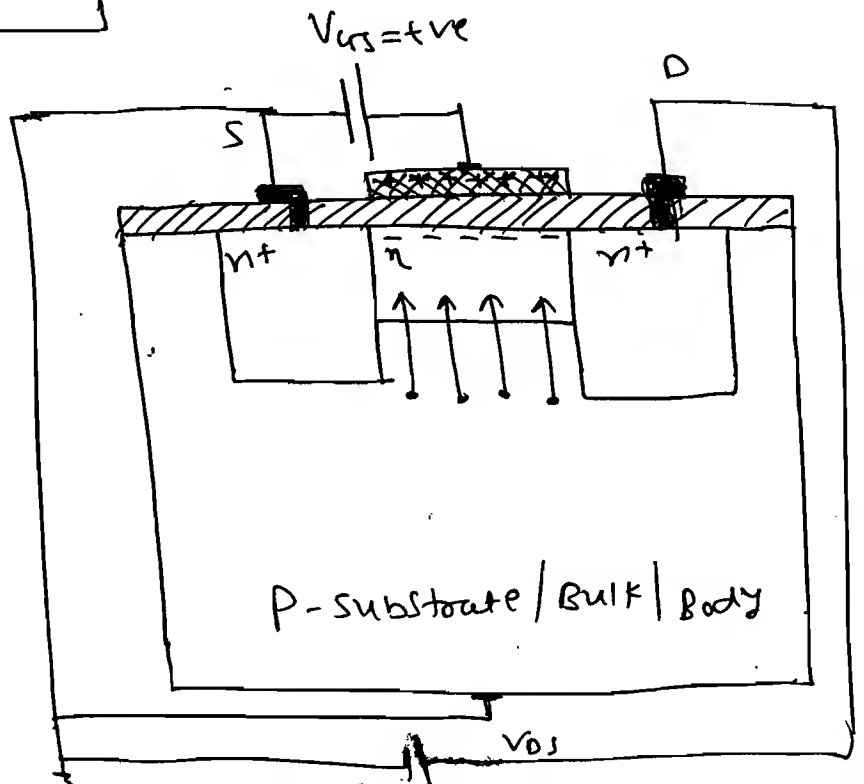
Case - (i):  $V_{GS} = 0$ .



$$E = \frac{V_{DS}}{L}$$

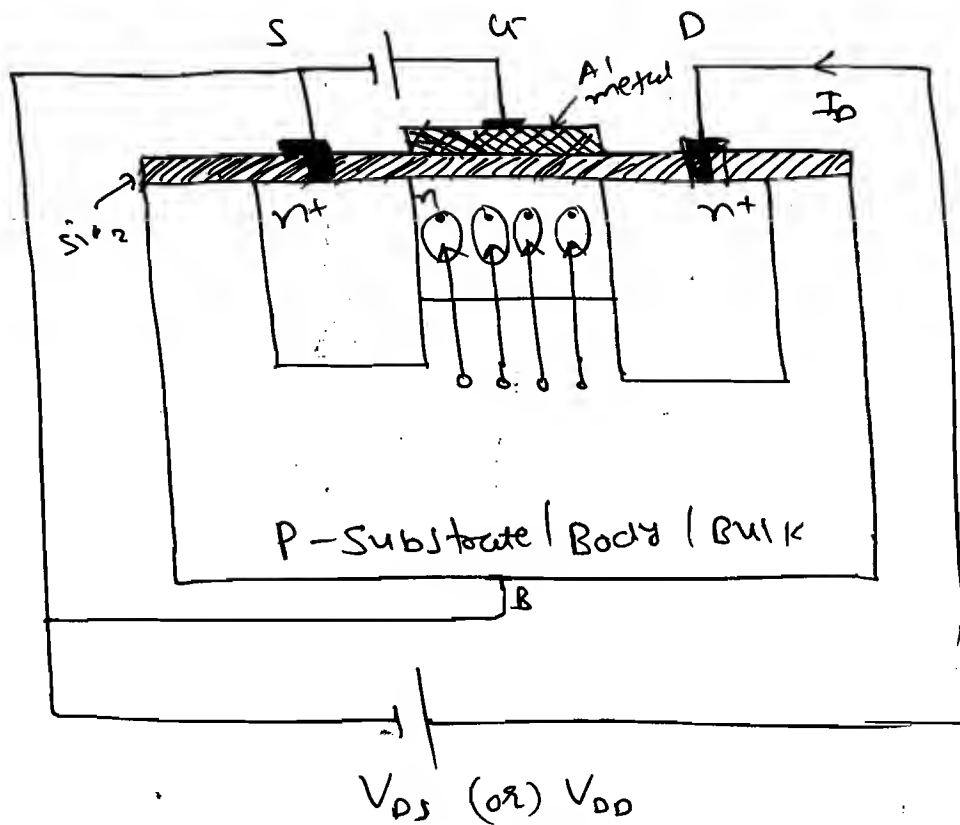


Case - (ii)  $V_{GS} = +ve$ .

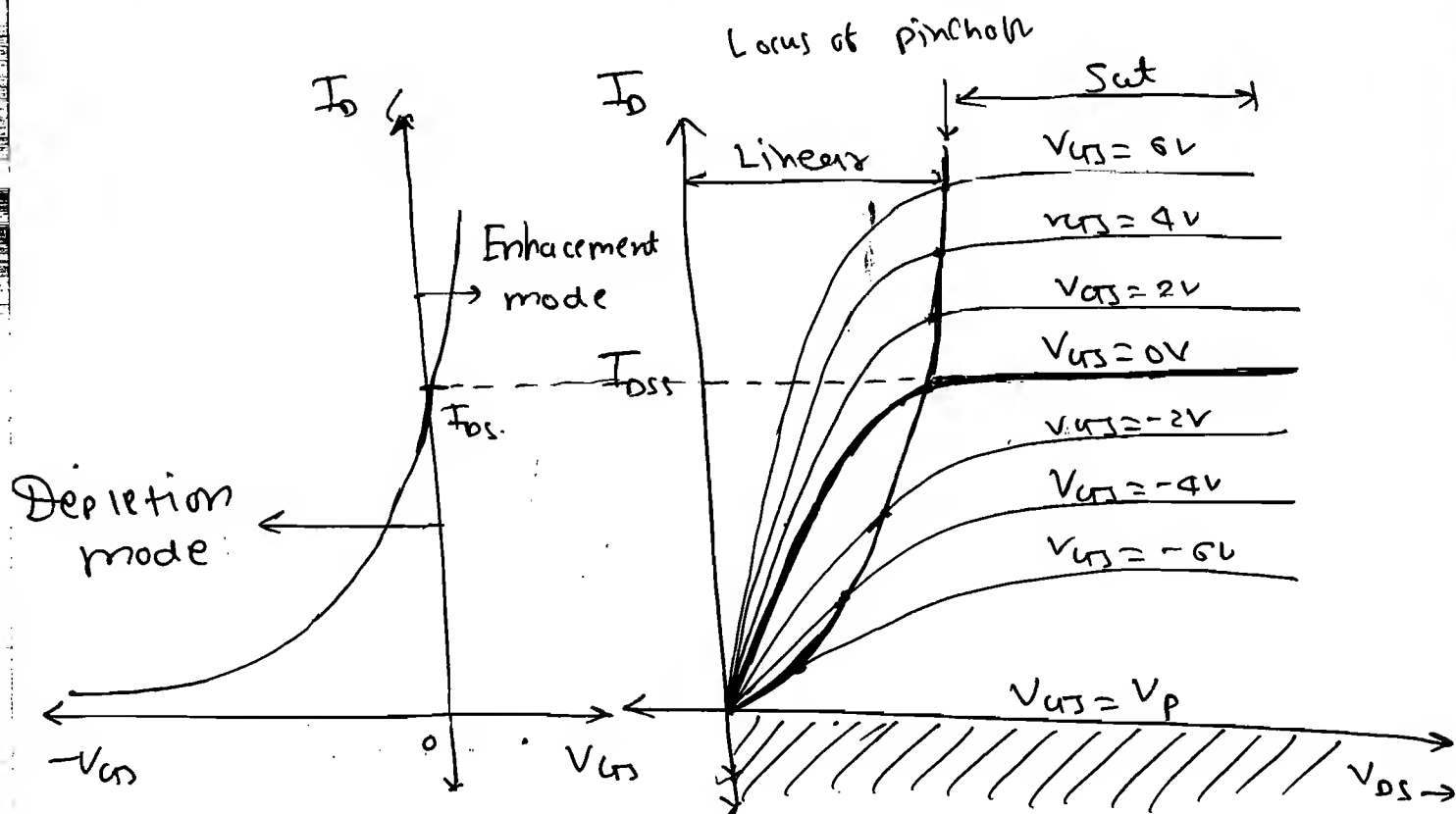


Case-(iii)

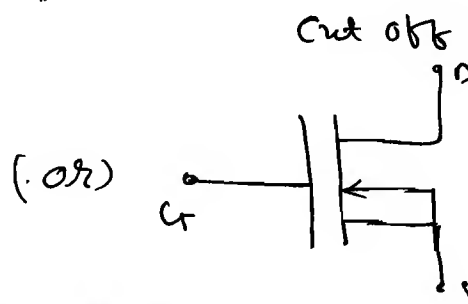
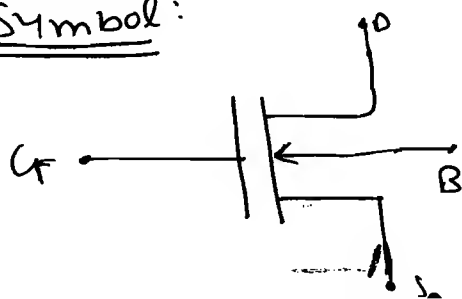
$V_{GS} = -ve$



\* Drain and Transfer Characteristics:



\* Symbol:





⇒ Important Points to be remember:

⇒ Pinch-off Voltage is -ve for n-channel DMOSFET.

⇒ n-channel Depletion MOSFET operates in enhancement mode for +ve  $V_{GS}$  value and it operates in depletion mode for -ve  $V_{GS}$  value.

⇒ Depletion Mos-FET operates in depletion and enhancement mode.

⇒ In discrete n-Channel DMOSFET Substrate (or) Body (or) Bulk is connected to the ground (or) Source terminal. Where as in IC's it should be connected to Most -ve voltage.

⇒ n-Channel depletion MOSFET will be on for +ve  $V_{GS}$  value and it will be OFF for -ve  $V_{GS}$  value (i.e.  $V_{GS} \leq V_p$ ).

⇒ Condition for pinch-off (or) ~~sat~~ Sat. is

$$\begin{array}{ccccc} V_{DS} = & V_{GS} & - & V_p & \\ \uparrow & \uparrow & & \uparrow & \\ +ve & +ve \text{ (or) } & & -ve & \\ & -ve & & & \end{array}$$

⇒ Transfer characteristics of a depletion MOSFET gives pinch-off Voltage ( $V_p$ ),  $I_{DSS}$  and transconductance  $g_m$ .

$\Rightarrow$  For  $V_{GS} \leq V_P$  operates in Cut-off region and its drain current  $I_D = 0$ .

$\Rightarrow$  For  $V_{GS} < V_{GS} - V_P$  it operates in linear region and its drain current

$$I_D = K_n [ 2 (V_{GS} - V_P) V_{DS} - V_{DS}^2 ]$$

$$K_n = \text{Constant} = \frac{I_{DSS}}{V_P^2} A V^2.$$

$$\therefore I_D = \frac{2 I_{DSS}}{V_P^2} \left[ \begin{array}{ccc} (V_{GS} - V_P) & V_{DS} & - \frac{1}{2} V_{DS}^2 \\ \uparrow \quad \uparrow \quad \uparrow \\ (+ve \text{ or } -ve) & -ve & +ve \end{array} \right].$$

$\Rightarrow$  for  $V_{GS} \geq (V_{GS} - V_P)$  it operates in Saturation region and its drain current

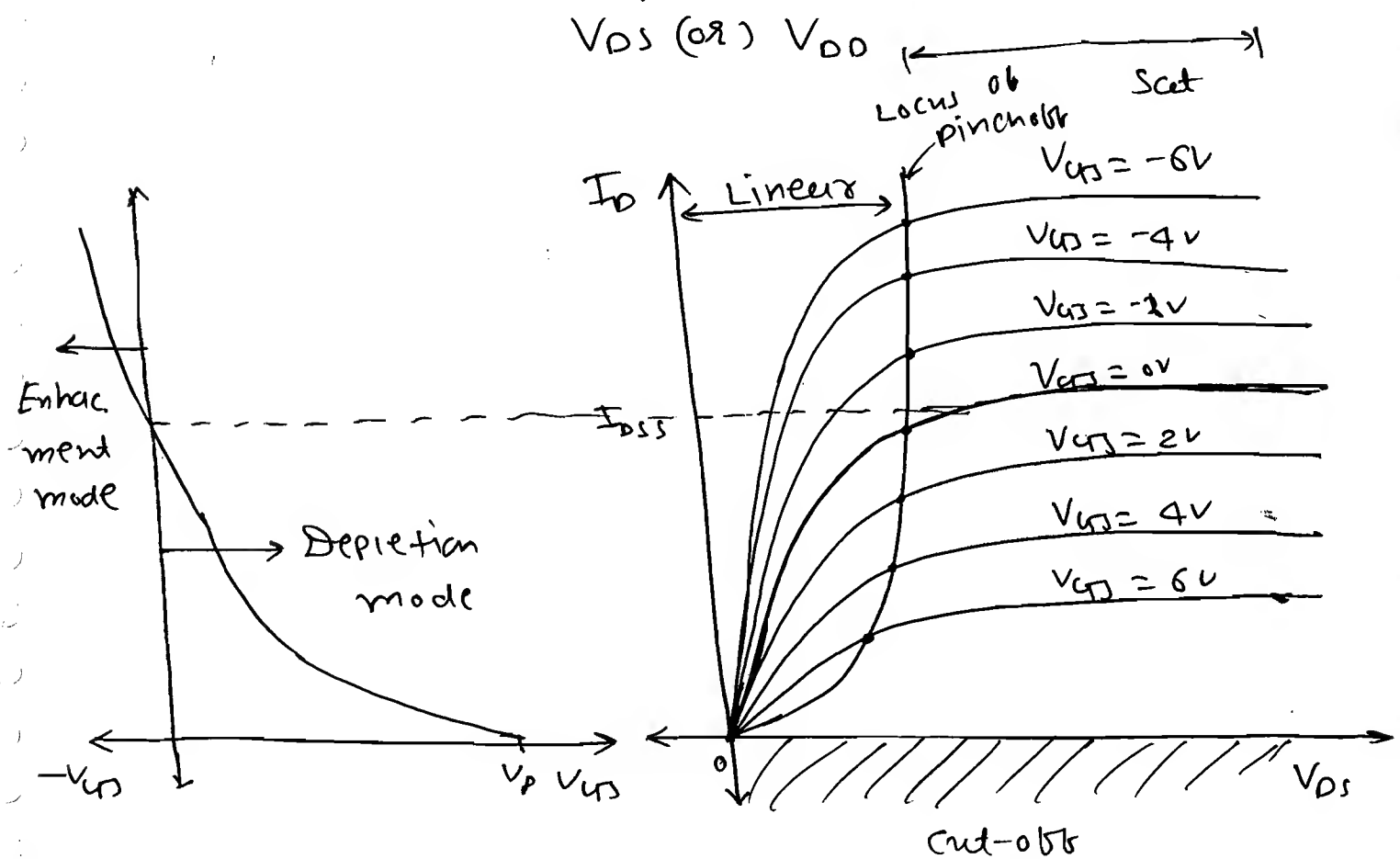
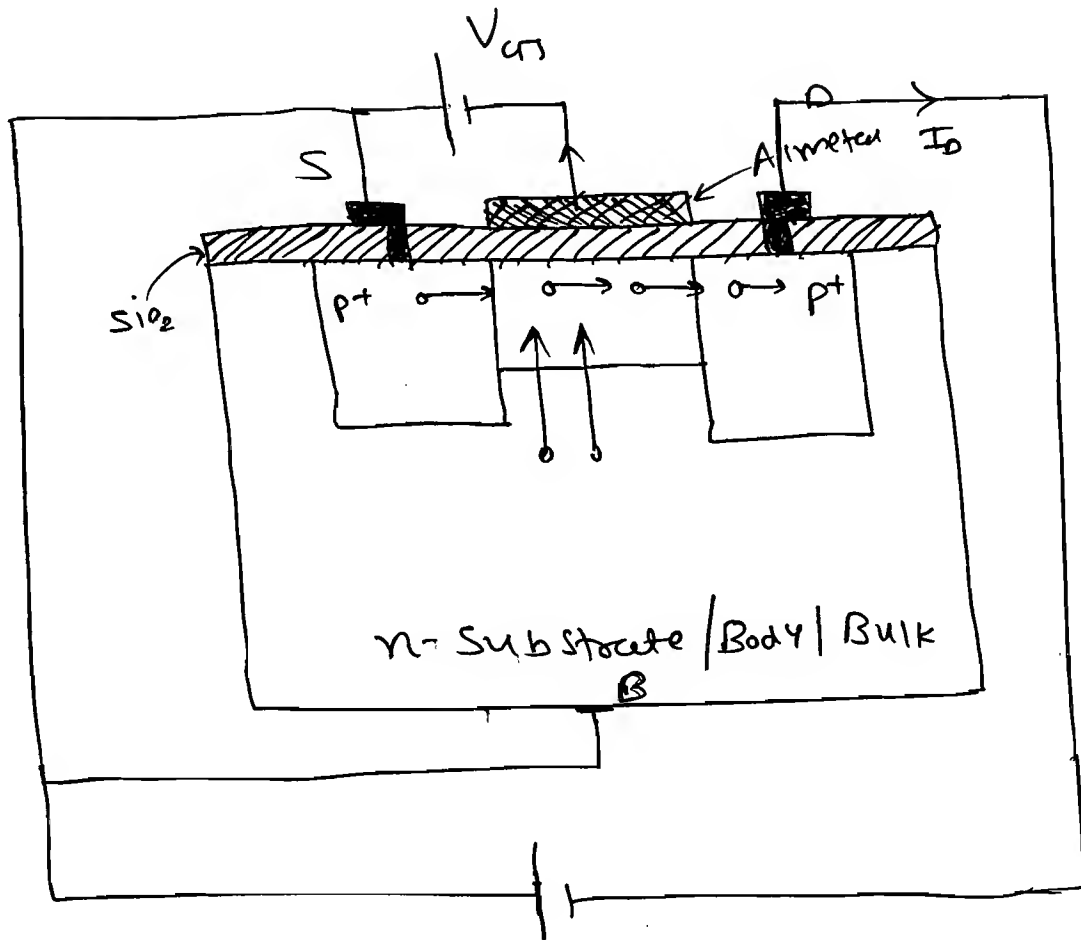
$$I_D = K_n [ V_{GS} - V_P ]^2, \quad K_n = \frac{I_{DSS}}{V_P^2} A V^2$$

$$\therefore I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$$

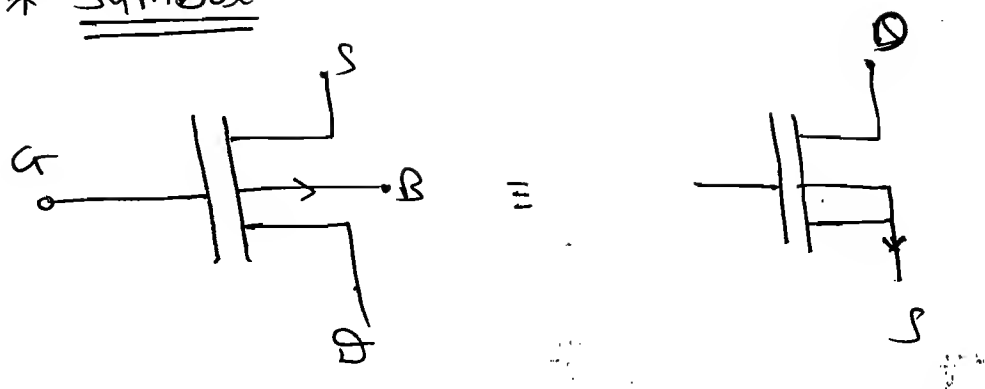
true or -ve.      -ve.

# ★ P-channel Depletion MOSFET:

46



\* Symbol:



\* Imp. points to be remember:

⇒ P-channel depletion MOSFET operates with  $+ve$  as well as  $-ve$   $V_{GS}$  value.

⇒ pinch-off voltage is  $+ve$  for P-MOSFET

⇒ P-channel depletion MOSFET operates in depletion mode for  $+V_{GS}$  and it operates in enhancement mode for  $-V_{GS}$  value.

⇒ In discrete P-D MOSFET Substrate (or) Body (or) Bulk should be connected to the ground (or) source terminal. whereas in IC's it should be connected to the most  $+ve$  voltage.

⇒ P-D MOSFET will be ON for  $-ve$   $V_{GS}$  values and it will be OFF for  $+ve$  values (i.e.  $V_{GS} \geq V_p$ ).

⇒ Condition for pinch-off (or) Saturation

$$-ve \rightarrow V_{DS} = V_{GS} - V_p \leftarrow +ve$$

$\uparrow$   
+ve or -ve

$\Rightarrow$  For  $V_{GS} \geq V_P$  P-DMOSFET operates in cut-off region and its drain current

$$I_D = 0.$$

$\Rightarrow$  For  $V_{GS} > V_{GS} - V_P$  it operates in linear region and its drain current is given by,

$$I_D = K_P [2(V_{GS} - V_P)V_{DS} - V_{DS}^2].$$

$$K_P = \frac{I_{DSS}}{V_P^2}.$$

$$\therefore I_D = \frac{2I_{DSS}}{V_P^2} \left[ \underset{\substack{\uparrow \\ +ve \text{ (or)} \\ -ve}}{(V_{GS} - V_P)} \underset{\substack{\uparrow \\ +ve}}{V_{DS}} - \underset{\substack{\uparrow \\ +ve}}{\frac{1}{2} V_{DS}^2} \right].$$

$\Rightarrow V_{DS} \leq V_{GS} - V_P$  it operates in Saturation region and drain current,

$$I_D = K_P [V_{GS} - V_P]^2.$$

$$\therefore I_D = \frac{I_{DSS}}{V_P^2} [V_{GS} - V_P]^2.$$

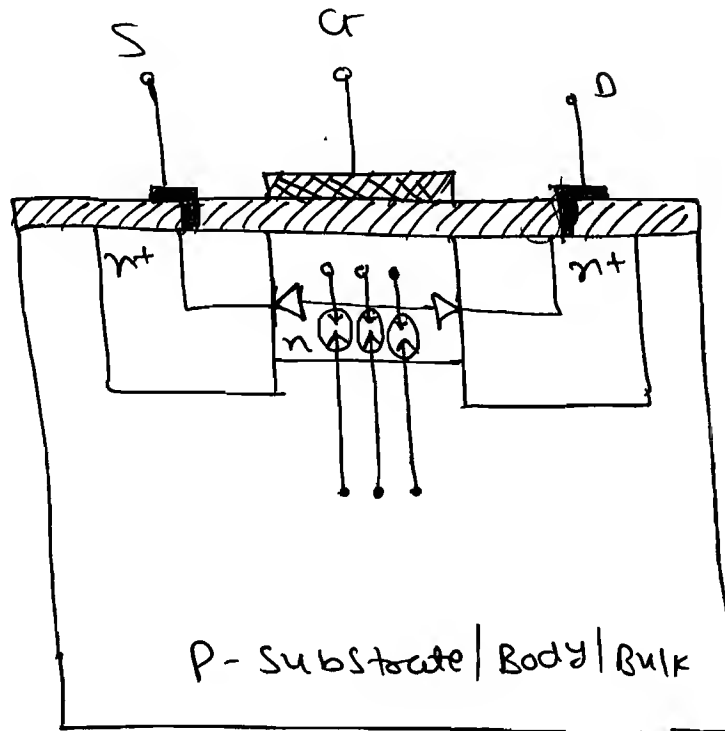
$$\therefore I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2 \quad \begin{matrix} +ve \text{ (or) } -ve \\ +ve. \end{matrix}$$

$\Rightarrow$  We prefer D-MOSFET for resistor instead of E-MOSFET.

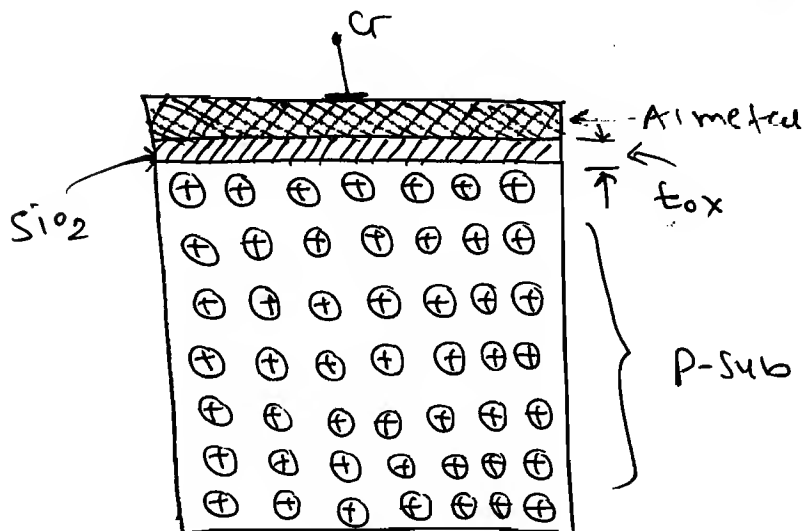
# ★ Enhancement MOSFET:

## ① n-Channel enhancement MOSFET: (n-EMOSFET)

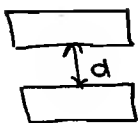
⇒



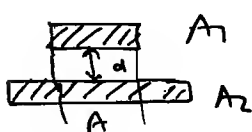
\*



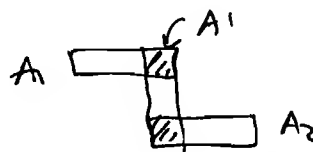
⇒



$$C = \frac{\epsilon A}{d}$$



$$C = \frac{\epsilon A_1}{d}$$



$$\epsilon C = \frac{\epsilon A_1}{d}$$

$$\Rightarrow \frac{C}{A} = \epsilon / d \quad \text{F/cm}^2 \quad (\text{or}) \quad \text{F/m}^2.$$

48)

$$\therefore \frac{C}{A} = \epsilon/d \quad \text{F/cm}^2 \text{ (or) } \text{F/m}^2.$$

$A$  = Common Area bet<sup>n</sup> two plate.

$\therefore C_{ox}$  = oxide Capacitor per ~~two~~ unit area

$$\therefore C_{ox} = \frac{\epsilon}{t_{ox}}.$$

$$\therefore \boxed{C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}} \quad \text{F/cm}^2 \text{ (or) } \text{F/m}^2.$$

$\Rightarrow t_{ox}$  : Gate oxide thickness

$\epsilon_{ox}$  : Permittivity of  $\text{SiO}_2$

$\epsilon_{ox} : \epsilon_{ox} \cdot \epsilon_0$  ,  $\epsilon_{ox}$  = relative Permittivity of  $\text{SiO}_2$

$$= 3.9 \approx 4 \checkmark$$

$$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m}$$

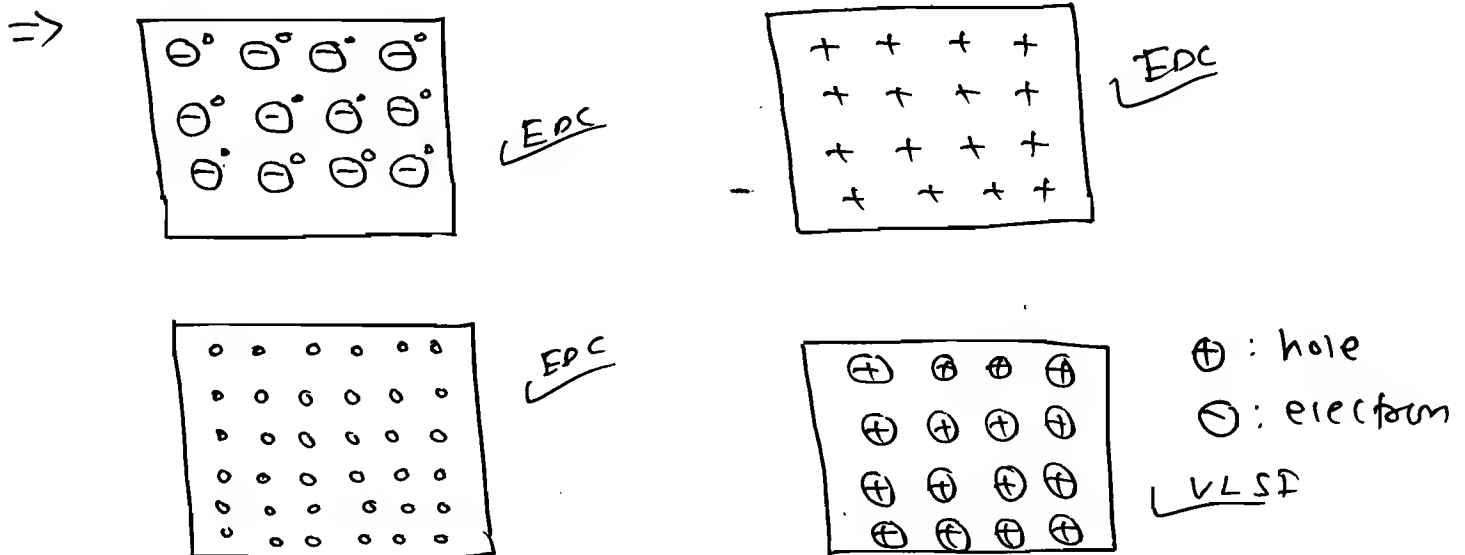
$$\epsilon_0 = 8.85 \times 10^{-14} \text{ F/cm.}$$

$$\therefore C_0 = C_{ox} \cdot A$$

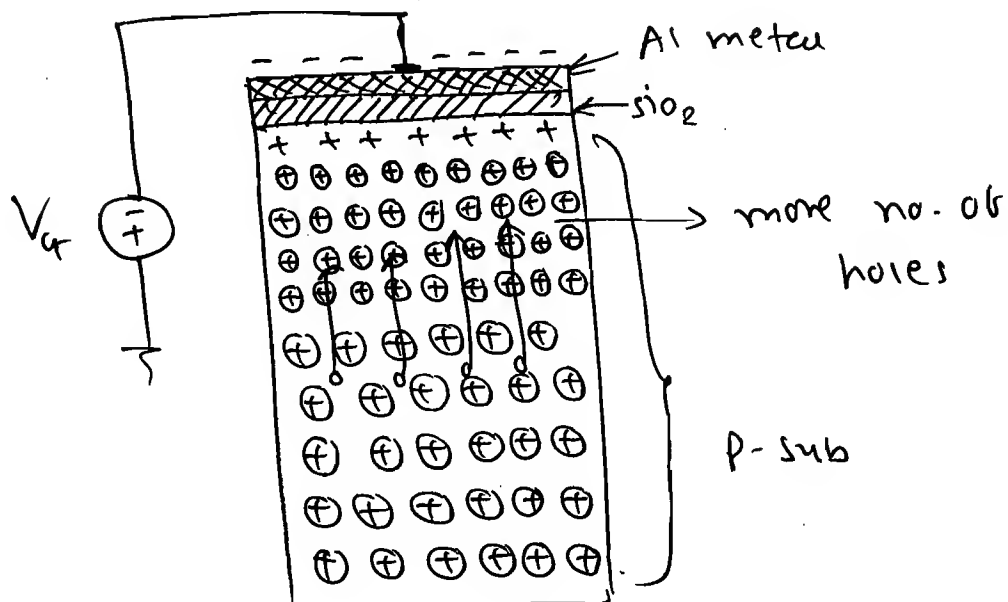
$$\therefore \boxed{C_0 = C_{ox} \times WL} \quad (\text{F})$$

$\therefore C_0$  = oxide Capacitance.

\* P-type representation:



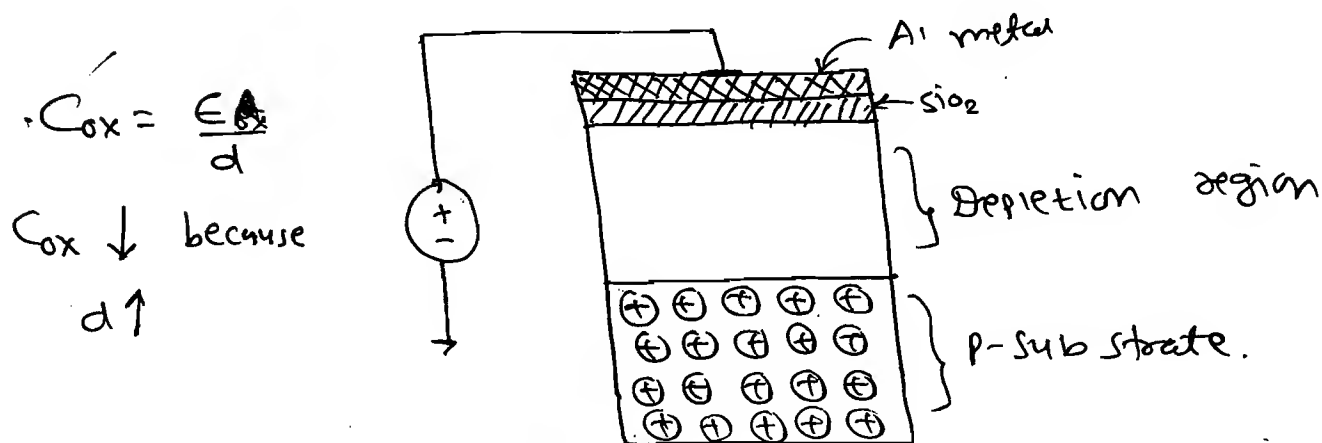
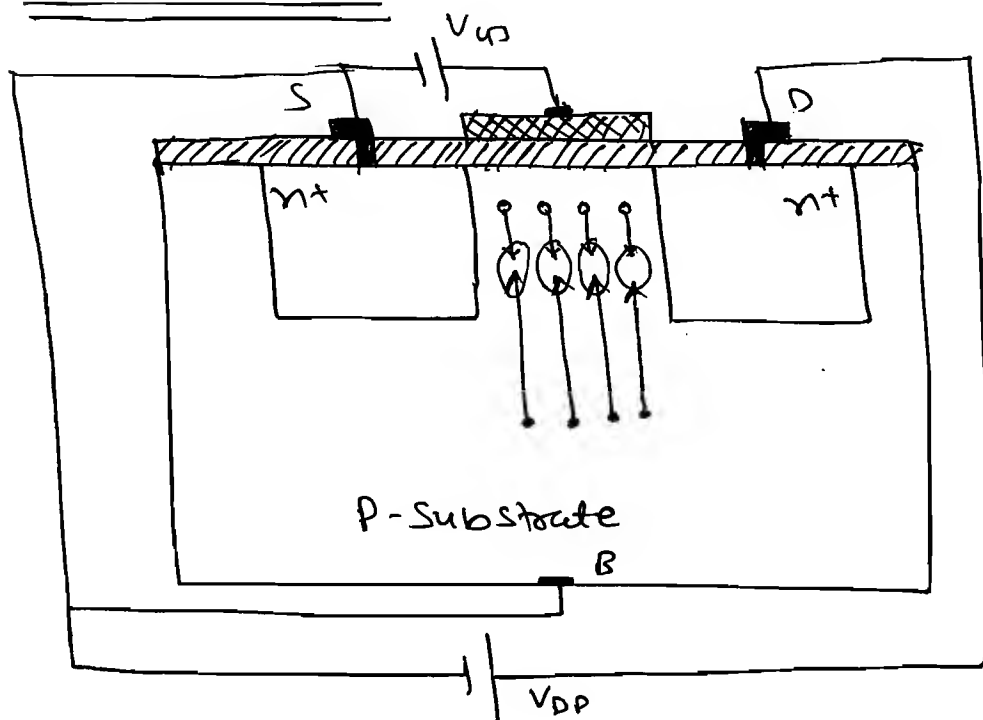
$$\Rightarrow \underline{V_{GS} = -V_e}$$



Accumulation mode.

$C_{ox}$  is same as that of for  $V_{GS} = 0V$ .

$$\Rightarrow \underline{0 < V_{GS} < V_T}$$



$$C_{ox} = \frac{\epsilon_0 \epsilon_r}{d}$$

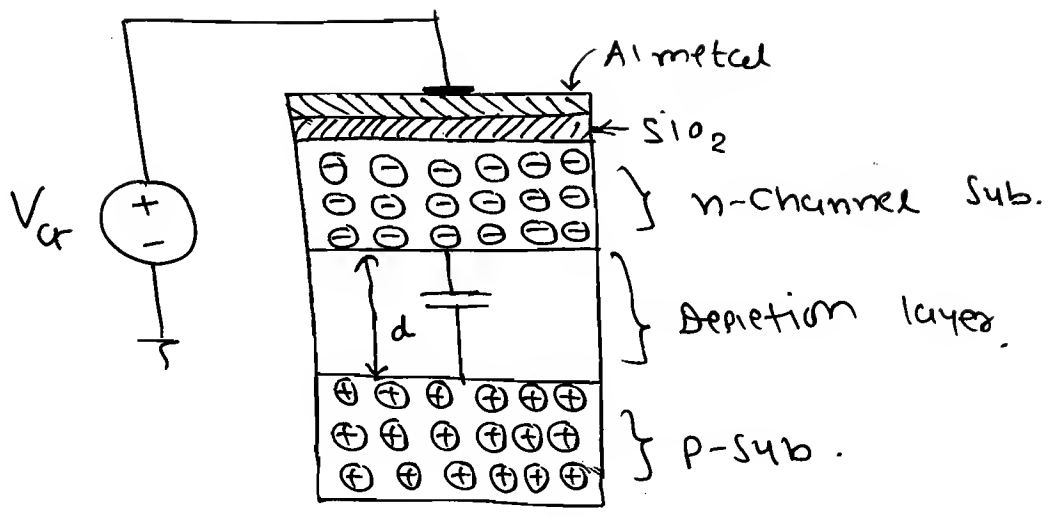
$C_{ox} \downarrow$  because  
 $d \uparrow$

Depletion mode.



③  $V_G > V_T$

⇒



( Inversion mode ).

⇒  ~~$R_{ox} = \frac{t_{ox}}{\sigma_{ox}}$~~

$C_{dep}$ : depletion Capacitance per unit area

$$C_{dep} = \frac{\epsilon_{si} \cdot A}{d} \quad \text{F/cm}^2 \text{ (or) } \text{F/m}^2$$

$\epsilon_{si}$ : Permittivity of silicon Si.

$d$ : Depletion layer thickness.

$\epsilon_{si} = \epsilon_{rsi} \cdot \epsilon_0$ ,  $\epsilon_{rsi} = 11.7 \approx 12$   
 $\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m}$

⇒  $C_d = C_{dep} \cdot A = C_{dep} \cdot W \times L$

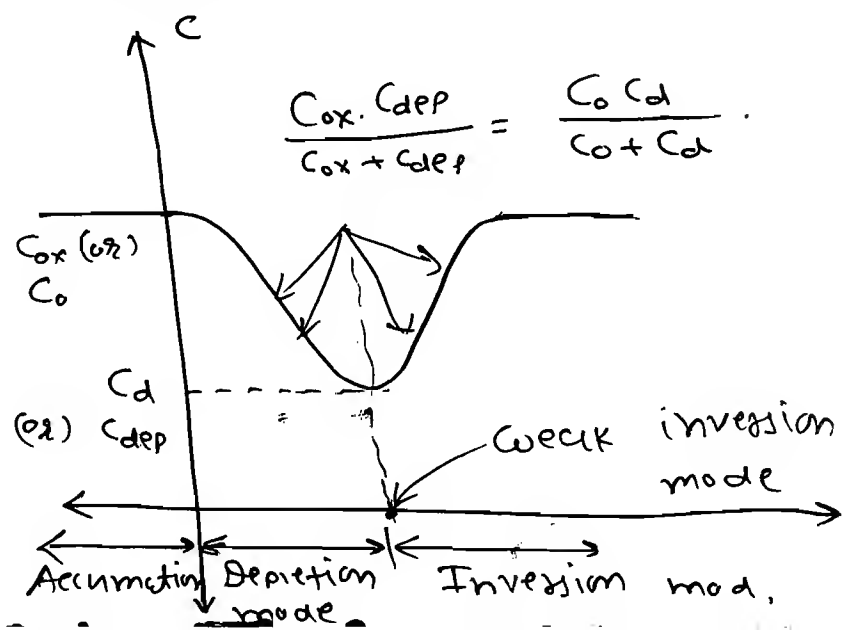
$C_d$ : depletion Capacitance.

⇒  $C_{eq} = \frac{C_{ox} \cdot C_{dep}}{C_{ox} + C_{dep}}$

∴  $C_{eq} = \frac{C_o \cdot C_d}{C_o + C_d}$

⇒ if  $t_{ox} \ll d$  Imp.

⇒  $\boxed{C_{ox} \gg C_{dep}} \\ \boxed{C_o \gg C_d}$



Here, ~~Cox = 7 PF~~  $C_0 = 7 \text{ PF}$

$$\therefore C_0 = \frac{\epsilon_0 \times A}{t_{ox}}$$

$$\therefore t_{ox} = \frac{3.5 \times 10^{-13} \times 10^{-4}}{7 \times 10^{-12}}$$

$$t_{ox} = 0.5 \times 10^{-5} \times 10^2 \text{ cm}$$

$$\therefore t_{ox} = 0.5 \times 10^{-3} \times 10^{-2}$$

$$\boxed{t_{ox} = 50 \text{ nm}}$$

$$\Rightarrow C_{eq} = \frac{C_d \cdot C_{ox}}{C_d + C_{ox}}$$

$$\therefore 1 = \frac{C_d \times 7}{C_d + 7}$$

$$\therefore C_d + 7 = 7 C_d$$

$$\therefore C_d = 7/6 \text{ PF}$$

$$C_d = \frac{\epsilon_{si} \cdot A}{d}$$

$$\therefore d = \frac{1 \times 10^{-12} \times 10^{-4}}{7/6 \times 10^{-12}} \times 6$$

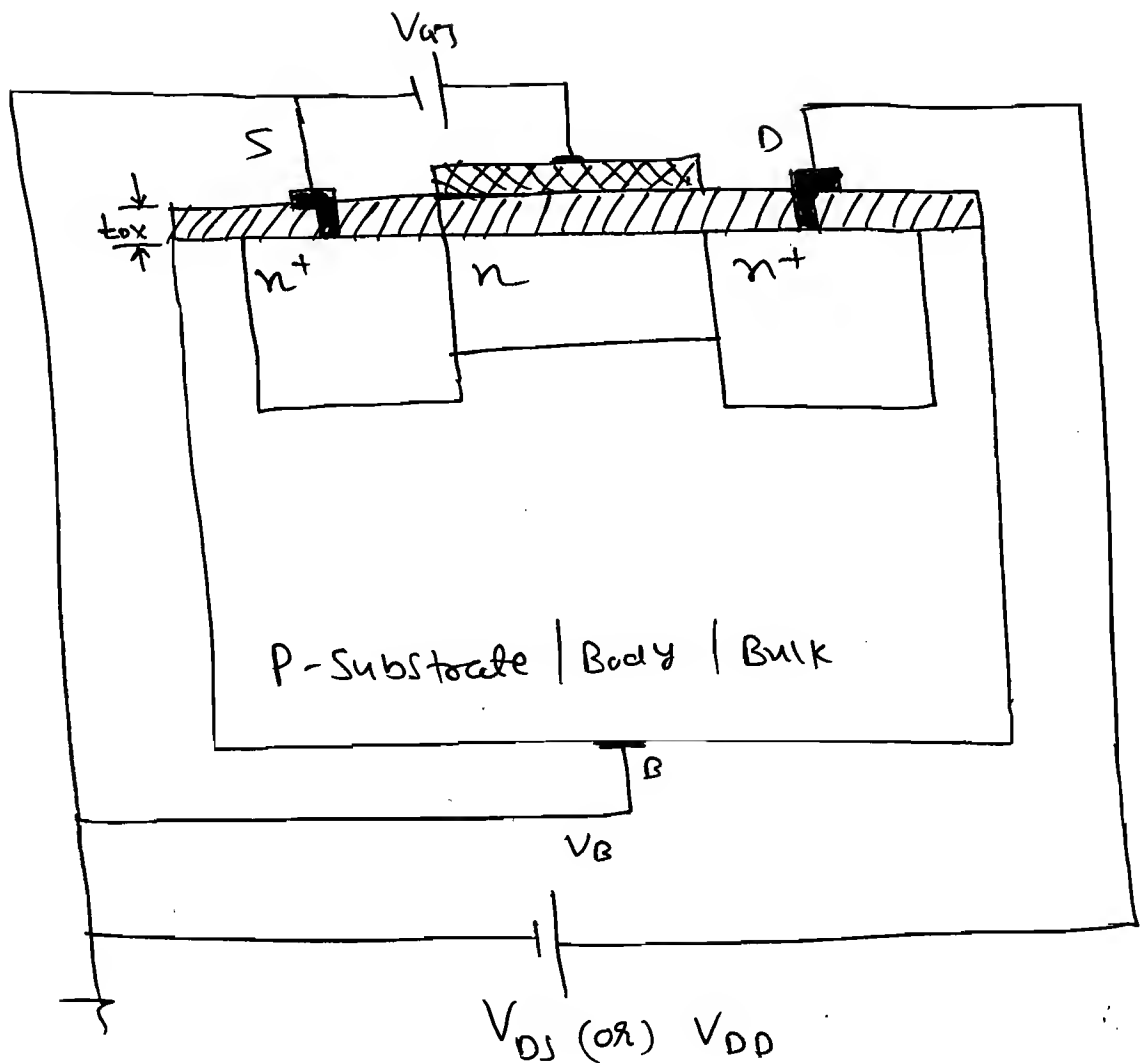
$$\therefore d = 0.143 \times 10^{-4} \text{ cm}$$

$$\therefore \boxed{d = 0.143 \mu\text{m}}$$

\* Threshold Voltage: ( $V_T$ ):

$\Rightarrow$  Threshold voltage is the minimum gate to source voltage required to accumulate sufficient no. of carriers and to form a channel bet<sup>n</sup> source and drain under the gate.

⇒



⇒

$t_{ox}$ : Gate oxide thickness.

$V_{SB}$ : Source to body voltage.

$N_A$  (or)  $N_D$ : Substrate doping density (or) Concentration.

⇒ Threshold Voltage depends on

- Gate oxide thickness ( $t_{ox}$ ).
- Source to body voltage ( $V_{SB}$ ).
- Substrate doping density (or) Concentration ( $N_A$  or  $N_D$ ).

→  $V_T : f(t_{ox}, V_{SB}, N_A \text{ (or) } N_D).$

⇒ Threshold Voltage of a MOSFET increases as gate oxide thickness

increases (or) it decreases as  $t_{ox}$  decreases.

$$\rightarrow t_{ox} \uparrow \rightarrow V_T \uparrow$$

$$t_{ox} \downarrow \rightarrow V_T \downarrow.$$

$\Rightarrow$  Threshold Voltage of a MOSFET is decreases as Source to Body Voltage decreases (or) it increases with increase in  $V_{SB}$ .

$$\Rightarrow V_{SB} \uparrow \rightarrow V_T \uparrow$$

$$V_{SB} \downarrow \rightarrow V_T \downarrow.$$

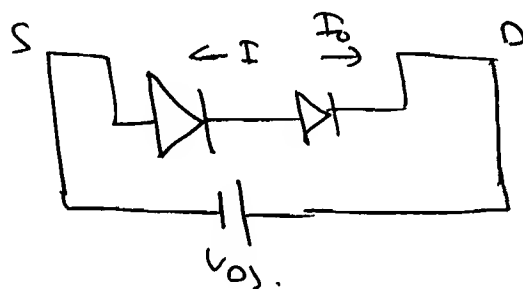
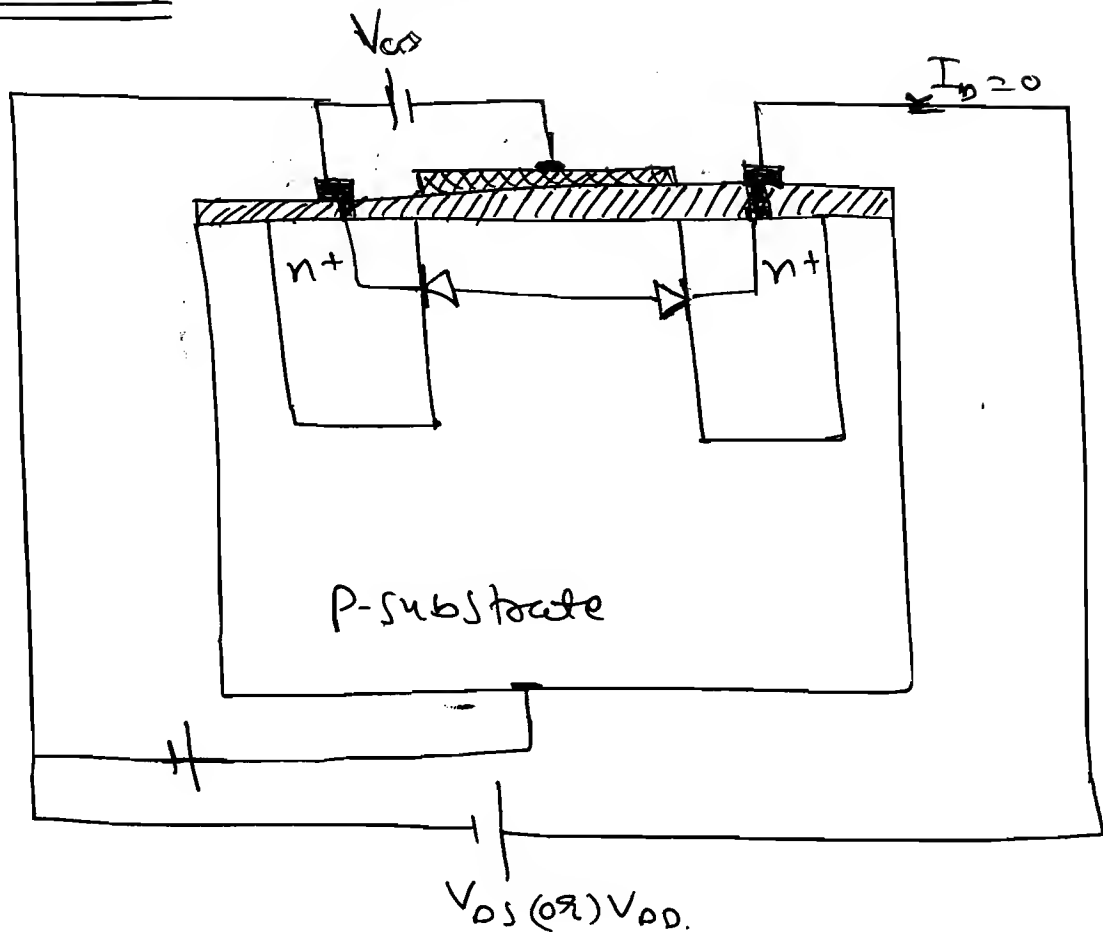
$\Rightarrow$  Threshold Voltage of a MOSFET increases as increases in doping density increases. (or) it decreases as substrate doping density decreases.

$$N_A \text{ (or) } N_D \uparrow \rightarrow V_T \uparrow$$

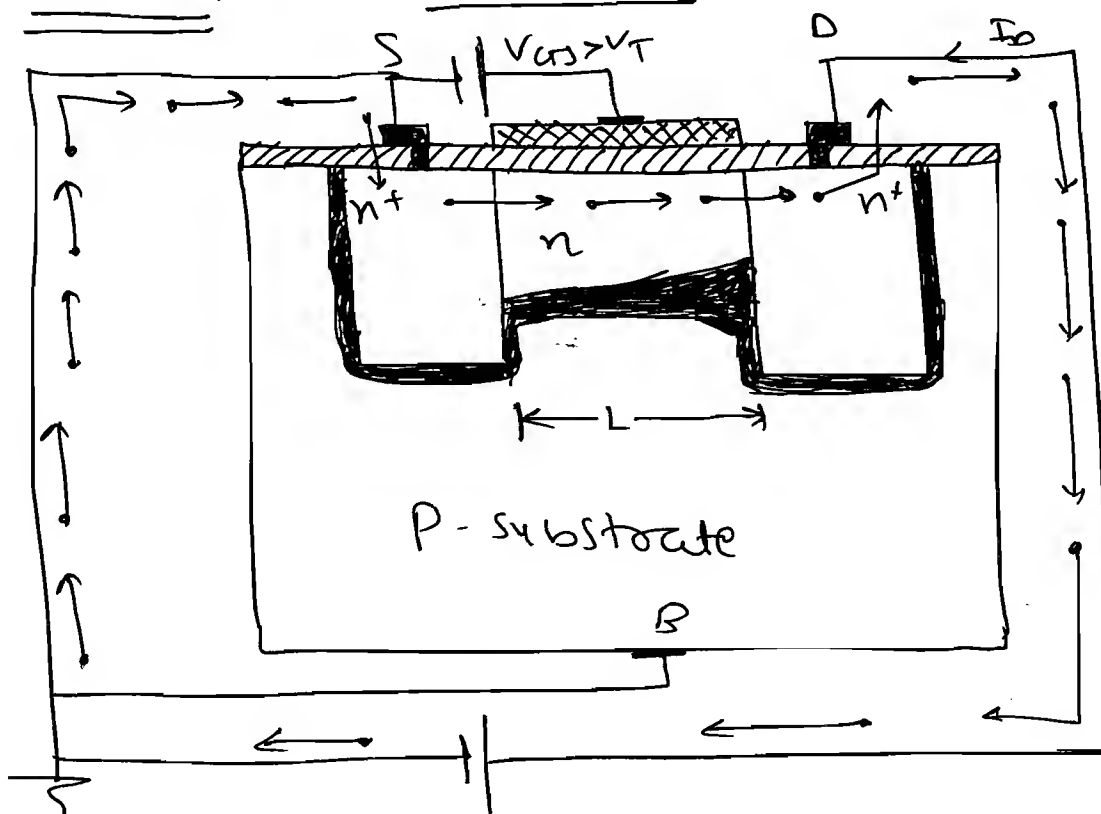
$$N_A \text{ (or) } N_D \downarrow \rightarrow V_T \downarrow.$$

$\Rightarrow$  Threshold Voltage is +ve for n-channel enhancement MOSFET and it is -ve for p-channel.

①  $V_{GS} < V_T$ : (cut-off).



②  $V_{GS} > V_T$  &  $V_{DS} < V_{GS} - V_T$ : (Linear):



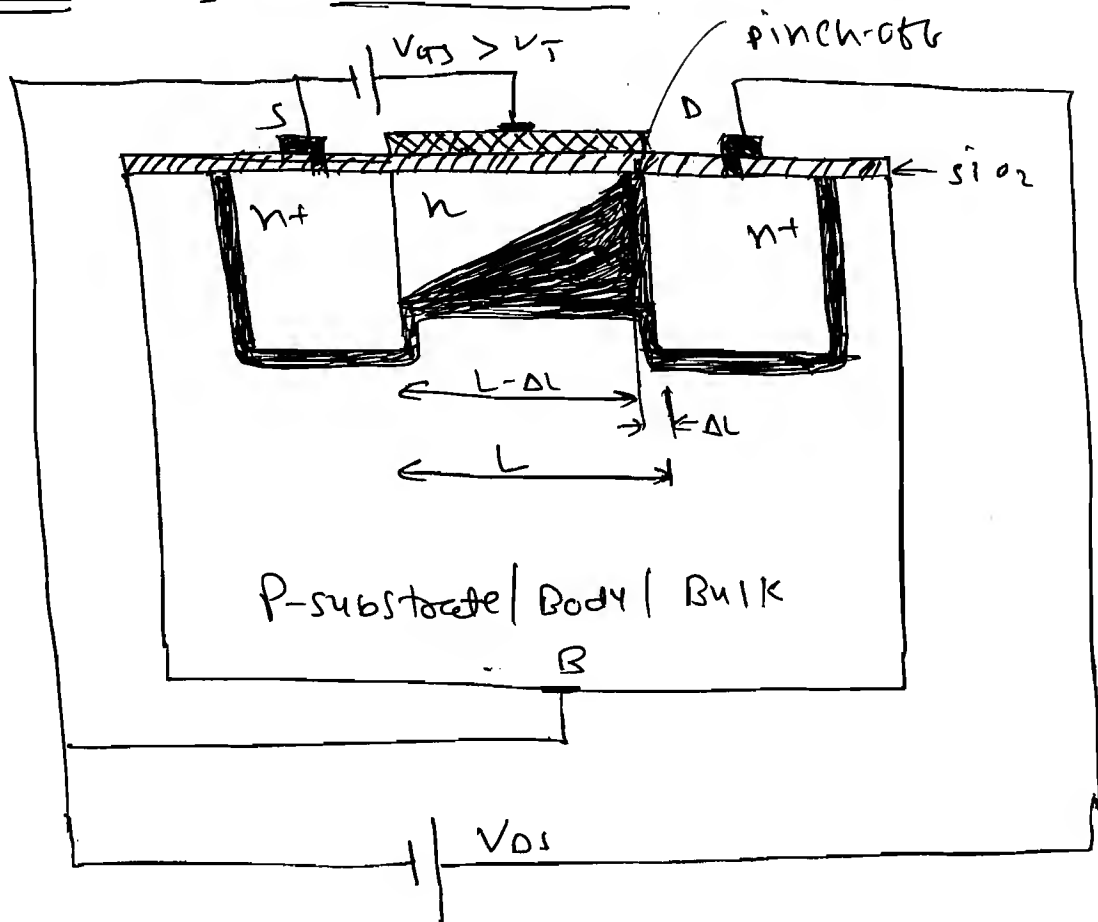
$$E = \frac{V_{DS}}{L}$$

$$V_{GS} = +V_G$$

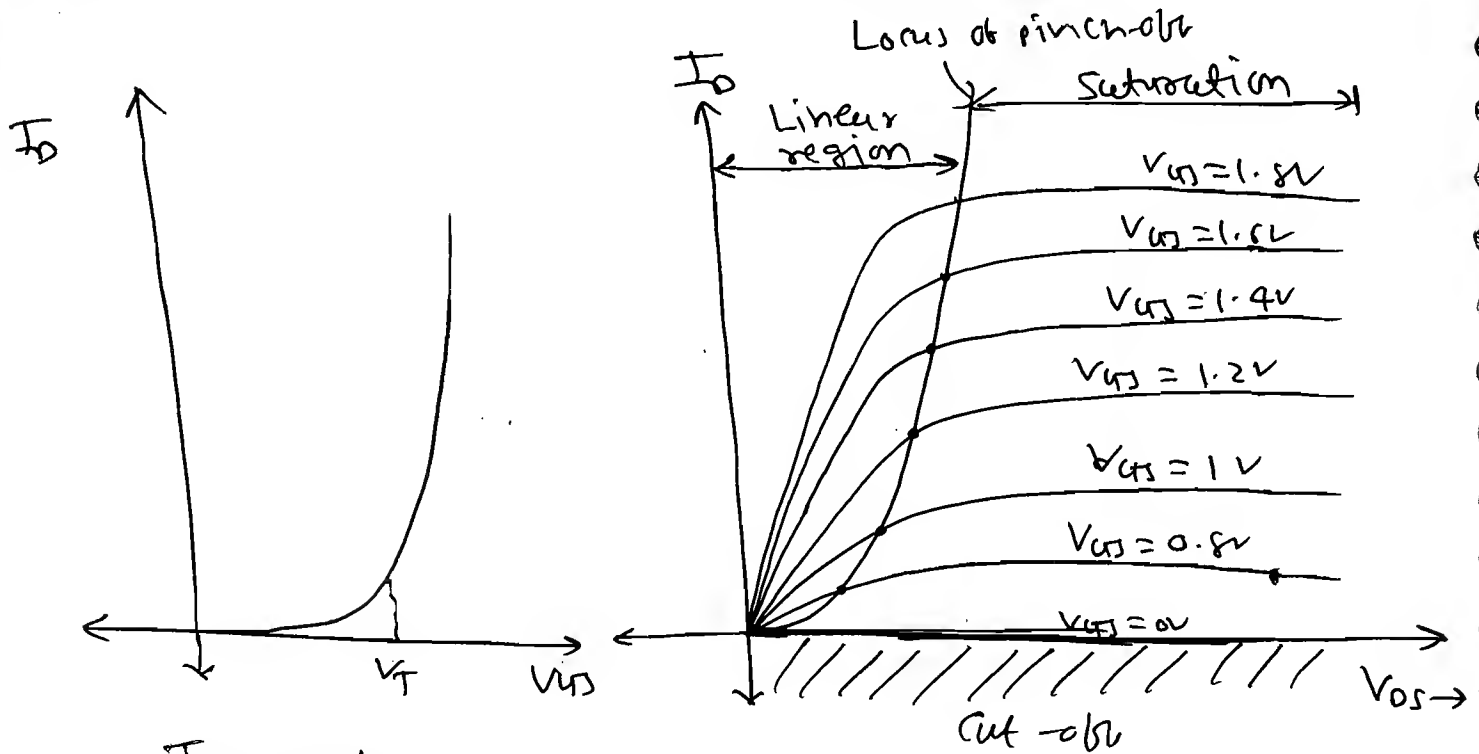
$$V_{DS} = +V_D$$

$$V_T = +V_P$$

(iii)  $V_{GS} > V_T$  &  $V_{DS} > V_{GS} - V_T$ . (Saturation):



\* Drain and transfer characteristics:



⇒ From drain characteristics,

we can only  $V_T$  &  $g_m$  can be extracted.

$\Rightarrow$  Channel Conductivity  $\propto (V_{GS} - V_T)$ .

$\Rightarrow$  Drain Current ( $I_D$ )  $\propto (V_{GS} - V_T)$ .

$\Rightarrow$

$V_{DS} = V_{GS} - V_T$

$\uparrow$                        $\uparrow$                        $\uparrow$   
 +ve                      +ve                      +ve.

$V_{DS} < V_{GS} - V_T$  : Linear

$V_{DS} > V_{GS} - V_T$  : Saturation.

$\Rightarrow$   $V_T$ ,  $V_{GS}$  &  $V_{DS}$ :

$\rightarrow$  if  $V_{GS} < V_T$  : cut-off.

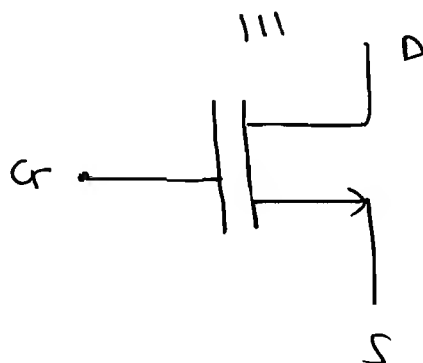
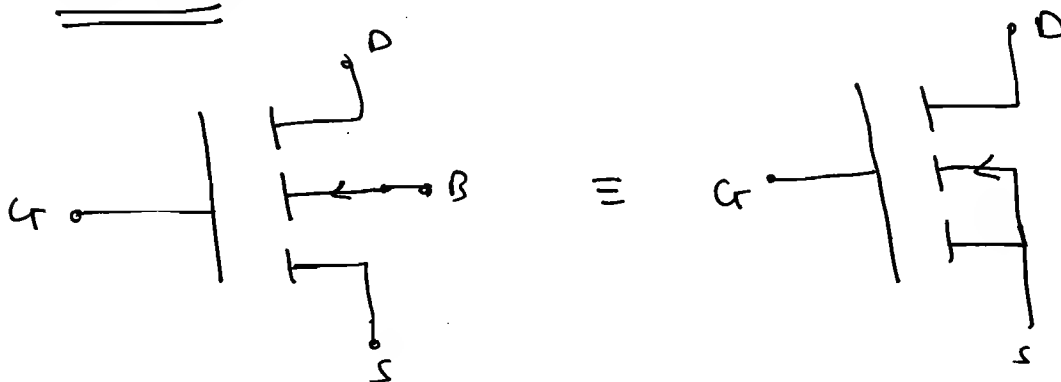
$\rightarrow$  if  $V_{GS} > V_T$

Calculate  $V_{GS} - V_T$ .

• if  $V_{DS} < V_{GS} - V_T$  : Linear

• if  $V_{DS} \geq V_{GS} - V_T$  : Saturation.

$\Rightarrow$  Symbol:



\* Important points to be remembered:

⇒ n-Channel E-MOSFET operates with +ve gate Voltages i.e. +ve  $V_{GS}$  value.

⇒ Gate to Source Voltage ( $V_{GS}$ ) and Threshold Voltage ( $V_T$ ) are +ve for n channel enhancement MOSFET.

⇒ n-EMOSFET operate in enhancement mode for +ve  $V_{GS}$  values.

⇒ n-EMOSFET always operates in enhancement mode.

⇒ In discrete n-Channel EMOSFET, Substrate (or) Body is Connected to the Ground or source terminal whereas in IC's it should be connected to the most -ve Voltage.

⇒ n-Channel EMOSFET will be on for +ve  $V_{GS}$  values (i.e.  $V_{GS} > V_T$ ) and it will be off for 0 (or) -ve  $V_{GS}$  values. (i.e.  $V_{GS} < V_T$ ).

⇒ At a given  $V_{GS}$  i.e. ( $V_{GS} > V_T$ ) as drain to Source Voltage increases the width of the drain depletion region increases.



→ At a particular value of  $V_{DS}$ , the thickness of the channel near to drain becomes zero it is called pinch-off. (52)

⇒ Condition for the pinch-off (or) sat is  $V_{DS} = V_{DS} - V_T$ . Here, all are +ve.

⇒ The Potential (or) Voltage across the channel increases from source to drain end, therefore the R.B. b/w channel and substrate increases from source to drain end.

⇒ The width of the depletion region bet<sup>n</sup> channel and substrate increases from source to drain end. Therefore the thickness of the channel decreases from source to drain end.

⇒ The inversion charge across the channel decreases from source to drain end.

⇒ At pinch-off (or) Saturation the channel is in tapered shape.

⇒ The electric field across the channel remain constant at pinch off (or) at saturation.

⇒ Linear region also called by Ohmic region (or) triode region.

⇒ Linear region is the region left side to the pinch-off locus.

⇒ Saturation region is the region right side to the locus of pinch-off.

⇒ Cut-off region is the region below the  $V_{GS} < V_T$ .

⇒ MOSFET can be operate as an Amplifier in Saturation and it can be operate as a switch in Linear and Cut-off region.

⇒ MOSFET can be used as a Voltage Variable Resistor <sup>in linear region</sup> and it can be used as a current source in the saturation region.

⇒ Transfer Characteristics of a E-MOSFET gives  $V_T$  &  $g_m$ .

⇒ For  $V_{GS} < V_T$ , n-EMOSFET operates in Cut-off region and its drain current  $I_D = 0A$ .

⇒ For  $V_{GS} > V_T$  &  $V_{DS} < V_{GS} - V_T$  it operates in linear region and its drain current  $I_D$  is,

$$\Rightarrow I_D = \mu_n C_{ox} \frac{W}{L} \left[ \underset{\substack{\uparrow \\ +ve}}{V_{GS}} - \underset{\substack{\uparrow \\ +ve}}{V_T} \right] \underset{\substack{\uparrow \\ +ve}}{V_{DS}} - \frac{1}{2} V_{DS}^2$$

→  $C_{ox}$ : Oxide Capacitance per unit area.

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$t_{ox}$ : Gate oxide thickness.

$\epsilon_{ox}$ : Permittivity of  $SiO_2$ .

$$\epsilon_{ox} = 3.9 \approx 4$$

$$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m.}$$

$$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/cm.}$$

⇒ For  $V_{GS} > V_T$  &  $V_{DS} \geq (V_{GS} - V_T)$  it operates in Sat. region and its drain current.

$$I_D = \frac{1}{2} \mu_n \cdot C_{ox} \cdot \frac{W}{L} \left[ \underset{\substack{\uparrow \\ +ve}}{V_{GS}} - \underset{\substack{\uparrow \\ +ve}}{V_T} \right]^2$$

Q - An n-channel enhancement MOSFET has  $V_T = 0.7 \text{ V}$ , and  $V_{GS} = 1.5 \text{ V}$ . Find the region of operation for  $V_{DS} = 2.5 \text{ volts}$ .

Sol<sup>n</sup>: Here,  $V_T = 0.7 \text{ V}$ ,  $V_{GS} = 1.5 \text{ V}$ .

$$V_{DS} = 2.5$$

$$\therefore V_{GS} > V_T$$

$$\text{and } V_{GS} - V_T = 1.5 - 0.7 = 0.8$$

$$\therefore V_{DS} > (V_{GS} - V_T = 0.8)$$

So, in Saturation.

Q - n-channel enhancement MOSFET has  $V_T = 0.7 \text{ V}$  and  $V_{GS} = 3 \text{ V}$ . Find the region of operation for  $V_{DS} = 2 \text{ V}$ .

Sol<sup>n</sup>:  $V_{GS} = 3 \text{ V}$ ,  $V_T = 0.7 \text{ V}$

$$V_{GS} > V_T$$

$$\& \quad V_{GS} - V_T = 3 - 0.7 = 2.3 \text{ V}$$

$$(V_{DS} = 2 \text{ V}) < (V_{GS} - V_T = 2.3 \text{ V})$$

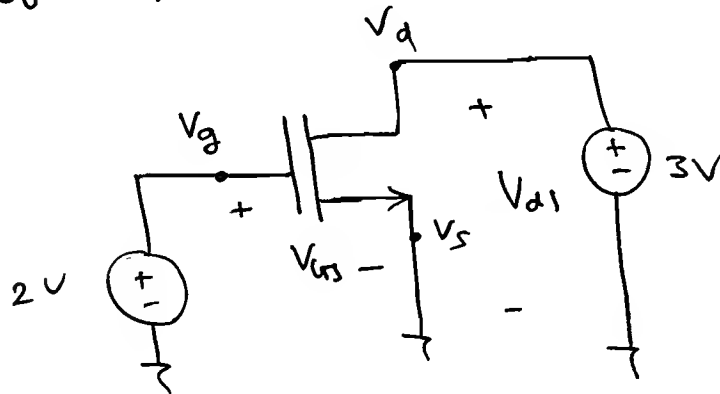
So, it operates in linear region.

Q: n-EMOSFET has  $V_{GS} = 1.2 \text{ V}$  &  $V_T = 1.5 \text{ V}$ . Find region of operation for  $V_{DS} = 4 \text{ V}$ .

Sol<sup>n</sup>:  $V_{GS} = 1.2 \text{ V}$ ,  $V_T = 1.5 \text{ V}$

$V_{GS} < V_T \Rightarrow$  it operates in cutoff region.

Q For the CKT Shown in the figure. MOSFET has threshold voltage  $0.6V$ . Find the region of operation.



Sol<sup>n</sup>:

By KVL  $2 - V_{gs} = 0$  &  $V_{ds} - 3 = 0$

$$\boxed{V_{gs} = 2V} \quad \boxed{V_{ds} = 3V}$$

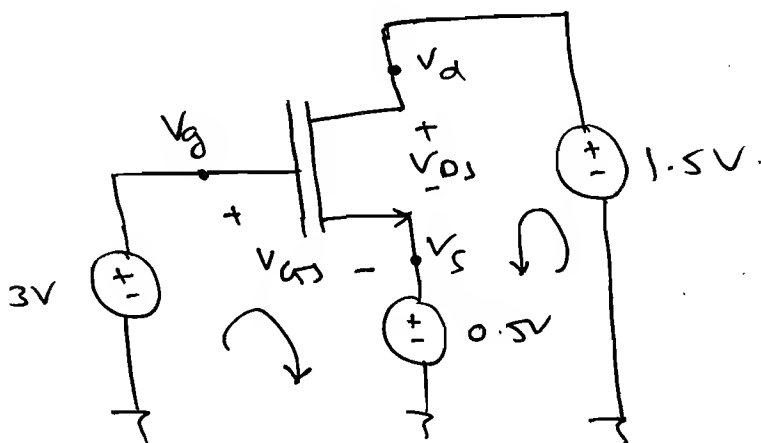
$V_T = 0.6V$

So,  $V_{gs} > V_T$  &  $V_{gs} - V_T = 2 - 0.6 = 1.4$

$\therefore V_{ds} > (V_{gs} - V_T = 1.4)$

So, it operates in Saturation.

Q For the CKT Shown in the fig. MOSFET has  $V_T = 0.6$ . Find the region of operation.



Sol<sup>n</sup>:

By KVL,

$3 - V_{gs} - 0.5 = 0 \Rightarrow$

$\boxed{V_{gs} = 2.5V}$

By KVL,  $1.5 - V_{ds} - 0.5 = 0$

$\Rightarrow \boxed{V_{ds} = 1V}$

&  $V_T = 0.6$  (given).

Now,  $V_{GS} = 2.5 > (V_T = 0.6V)$

$$V_{GS} - V_T = 2.5 - 0.6 = 1.9V$$

$$\therefore (V_{DS} = 1) < (V_{GS} - V_T) = 1.9$$

Therefore, it operates in linear region.

\* Imp:

① Linear:

$$\Rightarrow I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$\Rightarrow I_D = K_n' \cdot \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

Where,  $K_n' = \mu_n \cdot C_{ox} \cdot (A/V^2)$

$$K_n' = \frac{I_D}{(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2} \quad (A/V^2)$$

$$\Rightarrow I_D = \beta_n \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$\beta_n = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \quad A/V^2$$

$$\beta_n = K_n' \cdot \frac{W}{L} \quad A/V^2$$

$$\Rightarrow K_n' = K', \quad \beta_n = \beta = K$$

② Saturation:

$$\Rightarrow I_D = \frac{1}{2} \mu_n \cdot C_{ox} \cdot \frac{W}{L} [V_{GS} - V_T]^2$$

$$I_D = \frac{1}{2} \cdot K_n' \cdot \frac{W}{L} [V_{GS} - V_T]^2$$

$$\Rightarrow I_D = K_n [V_{GS} - V_T]^2$$

$$K_n = \frac{1}{2} \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (A V^2)$$

$$K_n = \frac{1}{2} K_n' \cdot \frac{W}{L} \cdot (A V^2)$$

$$I_D = \frac{1}{2} \beta_n [V_{GS} - V_T]^2, \quad \beta_n = \mu_n C_{ox} \cdot \frac{W}{L} \text{ (V/m}^2\text{)}$$

\* Deep Triode Region:

$\Rightarrow$  Deep triode region is also a linear region but for small values of  $V_{DS}$ .

$\Rightarrow$  Condition for Deep Triode Region is,

$$V_{DS} \ll 2[V_{GS} - V_T]$$

$$\Rightarrow I_D = \mu_n C_{ox} \cdot \frac{W}{L} \cdot [V_{GS} - V_T] V_{DS} - \frac{1}{2} V_{DS}^2$$

in linear region.

for deep triode region it is given by.

$$\therefore I_D = \mu_n C_{ox} \cdot \frac{W}{L} \times (V_{GS} - V_T) V_{DS}$$

$$I_D = K_n' \cdot \frac{W}{L} \times (V_{GS} - V_T) \cdot V_{DS}$$

$$I_D = \beta_n (V_{GS} - V_T) V_{DS}$$

$$\beta_n = \mu_n \cdot C_{ox} \times \frac{W}{L} = K_n' \cdot \frac{W}{L}$$

$$K_n' = \mu_n \cdot C_{ox}$$

$$\begin{aligned} K_n &= K = \beta_n \\ &= K_n' \cdot W/L \\ &= \mu_n \cdot C_{ox} \cdot \frac{W}{L} \end{aligned}$$

\* Drain ON Resistance (or) ON resistance  
 (or) Drain to Source resistance.

$\Rightarrow r_{ds(on)}, (or) r_{dson}, (or) R_{on}.$

$\Rightarrow$  Pinch-off point in drain characteristic  
 of MOSFET is  $\nabla$  called  $V_{DS}$  (or)  $V_{DSmin}$  (or)

$V_{DSsat}$  (or) over drive Voltage

$$\boxed{V_{ov} = V_{GS} - V_T.}$$

$\Rightarrow$  It is the resistance offered by the  
 MOSFET in the linear region for small  
 values of  $V_{DS}$ .

$\Rightarrow$  It is the reciprocal of the slope of  
 the drain characteristic in the linear  
 region for small value of  $V_{DS}$ .

$$r_{ds(on)} = r_{dson} = R_{on} = \frac{1}{\frac{\Delta I_D}{\Delta V_{DS}}}$$

$$\therefore \begin{array}{|l} R_{on} = \frac{\Delta V_{DS}}{\Delta I_D} \bigg|_{V_{GS}} \\ R_{on} = \frac{dV_{DS}}{dI_D} \bigg|_{V_{GS}} \end{array}$$

$$\Rightarrow I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} [V_{GS} - V_T] V_{DS}.$$

$$\therefore \frac{dI_D}{dV_{DS}} = \mu_n \cdot C_{ox} \cdot \frac{W}{L} (V_{GS} - V_T).$$



$$\therefore R_{on} = r_{d(ON)} = r_{ds(ON)} = \frac{1}{\mu_n C_{ox} \cdot \frac{W}{L} (V_{GS} - V_T)}$$

$$= \frac{1}{K_n' \cdot \frac{W}{L} (V_{GS} - V_T)}$$

$$= \frac{1}{\beta_n \cdot (V_{GS} - V_T)}$$

$$\therefore \boxed{R_{on} \propto \frac{1}{(W/L)} \cdot C \propto \frac{W}{L}}$$

$(V_{GS} - V_T) = V_{OV}$   
overdrive voltage

### \* Trans Conductance ( $g_m$ ):

$\Rightarrow$  Trans Conductance is also called as mutual Conductance (or) Figure of merit.

$\Rightarrow$  It gives how effectively MOSFET converts the voltage changes at input to the corresponding current changes at the output in saturation region.

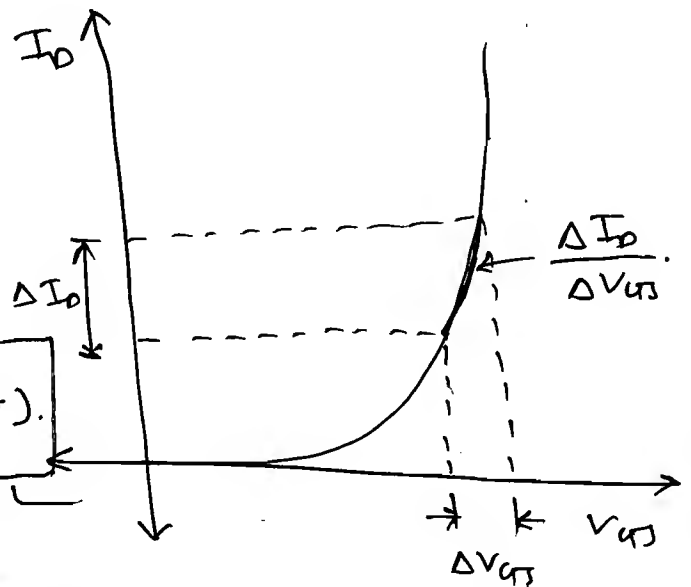
$\Rightarrow$  Trans Conductance is also equal to the slope of the transfer characteristics.

$$\Rightarrow I_D = \frac{1}{2} \mu_n C_{ox} \cdot \frac{W}{L} [V_{GS} - V_T]^2$$

$$\therefore \frac{dI_D}{dV_{GS}} = \mu_n C_{ox} \cdot \frac{W}{L} [V_{GS} - V_T]$$

$$\therefore \boxed{g_m = \frac{dI_D}{dV_{GS}} = \mu_n C_{ox} \cdot \frac{W}{L} (V_{GS} - V_T)}$$

$$\therefore \boxed{g_m = \frac{1}{R_{on}}}$$



- (1)

$$\Rightarrow \boxed{g_m = \sqrt{2 \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D}} \quad - (2) \quad - \textcircled{2}$$

$$g_m = 2 k_n (V_{GS} - V_T)$$

$$\Rightarrow g_m = \sqrt{2 \mu_n \cdot C_{ox} \cdot \frac{W}{L}} \cdot \sqrt{\frac{1}{2} \mu_n C_{ox} \times \frac{W}{L} \cdot (V_{GS} - V_T)^2}$$

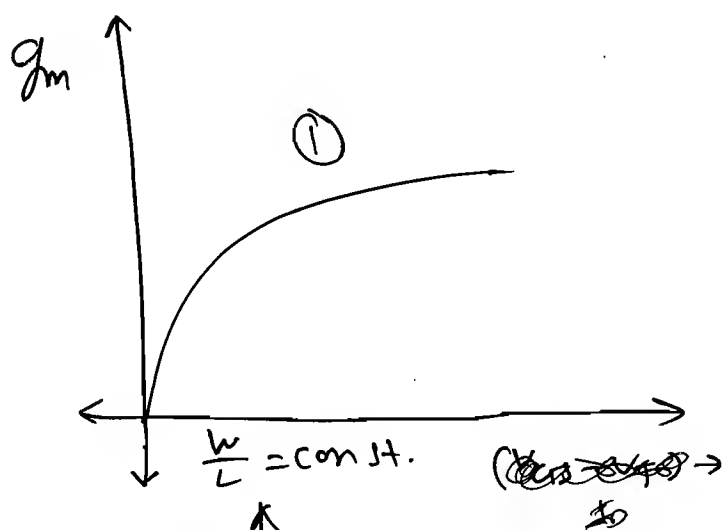
$$\therefore g_m = \sqrt{2 \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D} \quad (AIV)$$

$$\Rightarrow \boxed{g_m = \frac{2 I_D}{V_{GS} - V_T}} \quad - (3)$$

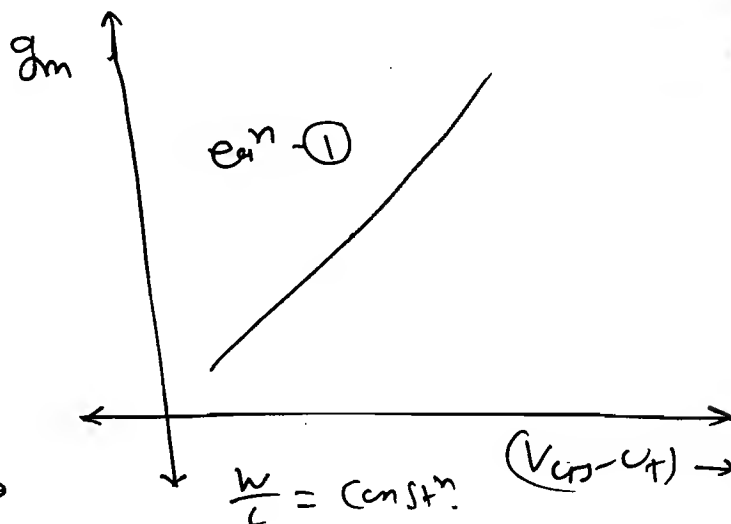
$$\rightarrow g_m = \frac{2 \cdot \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} (V_{GS} - V_T)^2}{(V_{GS} - V_T)}$$

$$\therefore \boxed{g_m = \frac{2 I_D}{V_{GS} - V_T}}$$

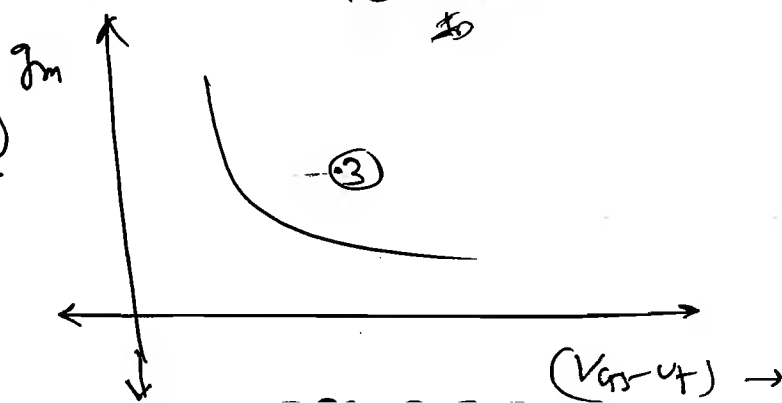
\* eqn-①



\* eqn-②

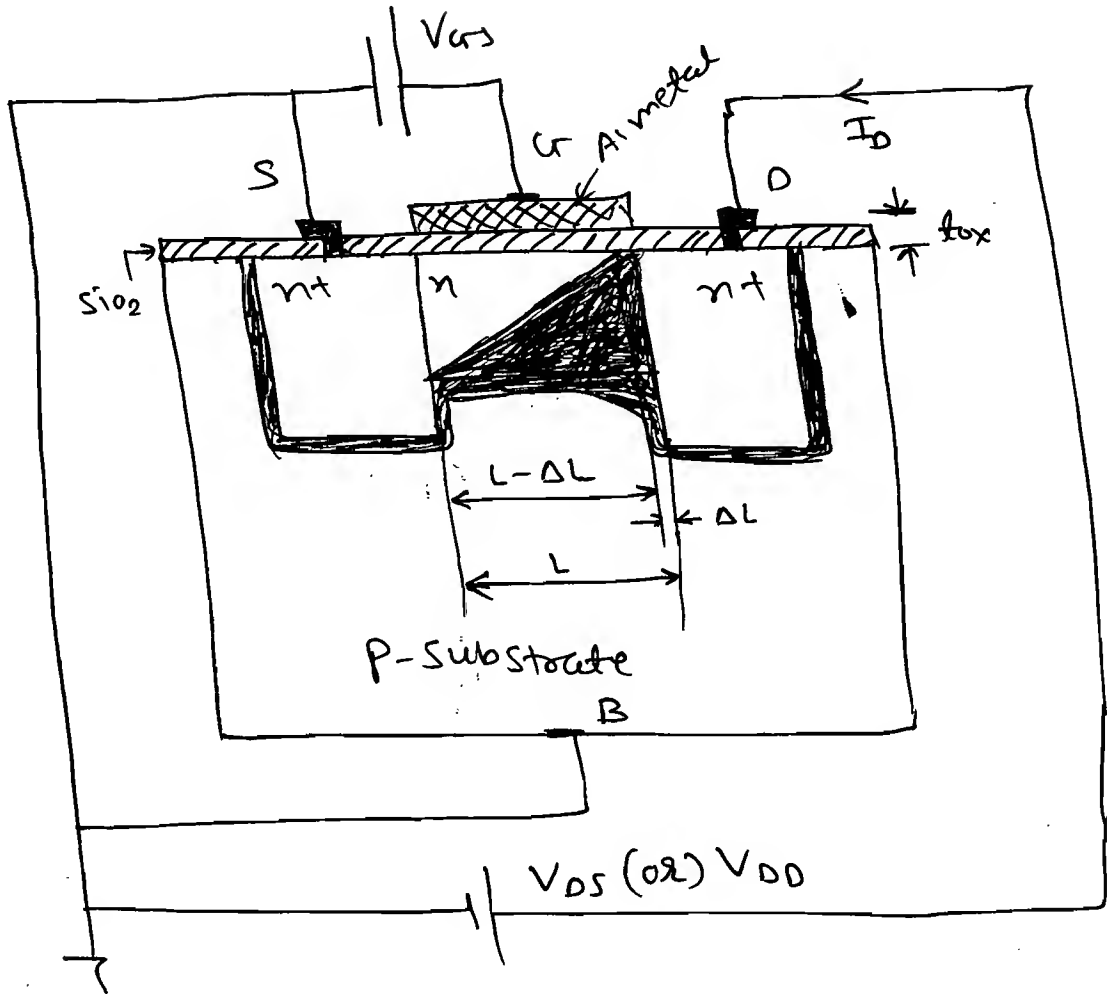


\* eqn-③



# \* Channel Length Modulation:

⇒

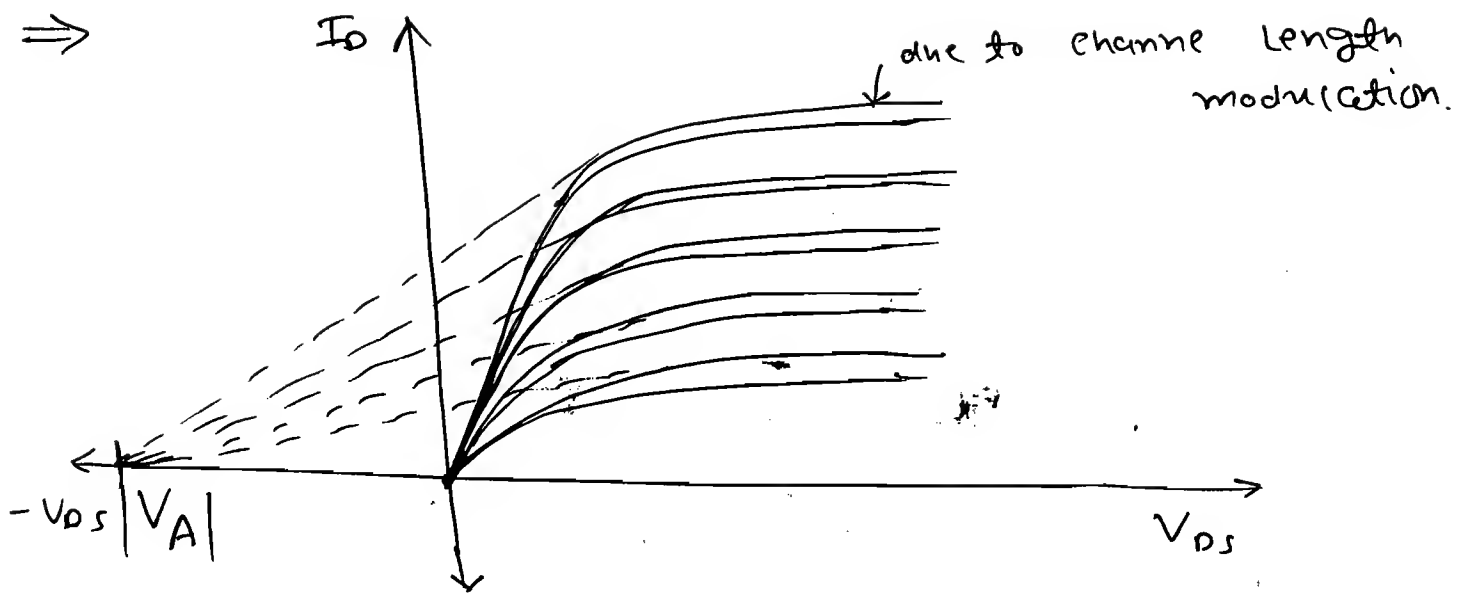


⇒ In the saturation region as drain to source increases the effective length of the channel decreases i.e. as  $V_{DS}$  varies the length of the channel is varied it is called channel length modulation.

⇒ Due to channel length modulation drain current increases and it is given by

$$I_D = \frac{1}{2} \mu_n \cdot C_{ox} \cdot \frac{W}{L} [V_{GS} - V_T]^2 (1 + \lambda V_{DS})$$

$\lambda = \frac{1}{V_A}$  ;  $V_A$  = Early Voltage.  $V_{A0} = V_{DS} - V_{DS} > V_T$   
 Required  $\rightarrow V_{A0} = V_{DS} - V_{DS} = V_T$



\* Drain Resistance (or) o/p resistance :  
 $r_d$  (or)  $r_o$  :

⇒ It is the resistance offered by the MOSFET in the saturation region.

⇒ It is the reciprocal of the slope of drain characteristics in the saturation region.

⇒ Slope =  $\left. \frac{\Delta I_D}{\Delta V_{DS}} \right|_{V_{GS}}$

$$r_d \text{ (or) } r_o = \left. \frac{1}{\frac{\Delta I_D}{\Delta V_{DS}}} \right|_{V_{GS}} = \left. \frac{\Delta V_{DS}}{\Delta I_D} \right|_{V_{GS}} = \left. \frac{dV_{DS}}{dI_D} \right|_{V_{GS}}$$

$$r_d \text{ (or) } r_o = \frac{1}{\lambda I_D}$$

⇒  $I_D = \frac{1}{2} \mu_n \cdot C_{ox} \cdot \frac{W}{L} [(V_{GS} - V_T)^2] (1 + \lambda V_{DS})$

$$\therefore \frac{dI_D}{dV_{DS}} = \underbrace{\frac{1}{2} \mu_n \cdot C_{ox} \cdot \frac{W}{L} [V_{GS} - V_T]^2}_{I_D \text{ (without channel length modulation)}} \cdot \lambda$$

$$\therefore \frac{dI_D}{dV_{DS}} = \lambda \cdot I_D.$$

$$\therefore r_{ds} \text{ (or) } r_o = \frac{1}{\lambda I_D} = \frac{V_A}{I_D} \quad \left( \because \lambda = \frac{1}{V_A} \right).$$

$\Rightarrow$  Drain resistance (or) O/P resistance is also called A.C. resistance (or) Small signal resistance.

\* Body effect:

$\rightarrow$  due to body effect  $V_T \uparrow$   
 $\Rightarrow V_{SB}$ : Source to Body Voltage.

$V_{TO}$ : Threshold Voltage of MOSFET when

$$V_{SB} = 0.$$

$$V_T = V_{TO} + \gamma \left[ \sqrt{V_{SB} + \phi_s} - \sqrt{\phi_s} \right].$$

$V_T$ : Threshold voltage of MOSFET at a given  $V_{SB}$ .

$\phi_s$ : Surface potential,  $\phi_s = 2V_T \ln \left( \frac{N_A}{n_i} \right).$

$V_T$ : Thermal voltage.

$$V_T = \frac{T}{11,600} = \frac{300}{11,600} = 0.02586 = 26 \text{ mV}.$$

$\gamma$ : Body effect Co-efficient.

$$\gamma = \frac{\sqrt{2qN_A \cdot \epsilon_{Si}}}{C_{ox}}, \quad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}.$$

$$\gamma = \frac{t_{ox}}{\epsilon_{ox}} \cdot \sqrt{2qN_A \epsilon_{Si}}.$$

$$\Rightarrow \begin{array}{l|l|l} t_{ox} \uparrow \rightarrow V_T \uparrow & V_{SB} \uparrow \rightarrow V_{SB} \uparrow & (N_A \text{ or } N_D) \uparrow \rightarrow V_T \uparrow \\ t_{ox} \downarrow \rightarrow V_T \downarrow & V_{SB} \downarrow \rightarrow V_{SB} \downarrow & (N_A \text{ or } N_D) \downarrow \rightarrow V_T \downarrow \end{array}$$

$\Rightarrow$  Due to body effect threshold voltage increases. Therefore drain current decreases.

\* Temperature effect:

$$\Rightarrow V_T \propto k_n' = \mu_n C_{ox}.$$

$\Rightarrow$  Case (i):  $V_T$

$V_T$  : dependent on Temperature.

$V_T$  : dec by  $2m/^\circ C$ .

$$T \uparrow \rightarrow V_T \downarrow \rightarrow I_D \uparrow$$

PTC

$\Rightarrow$  Case (ii):

$$\rightarrow k_n' = \mu_n C_{ox}.$$

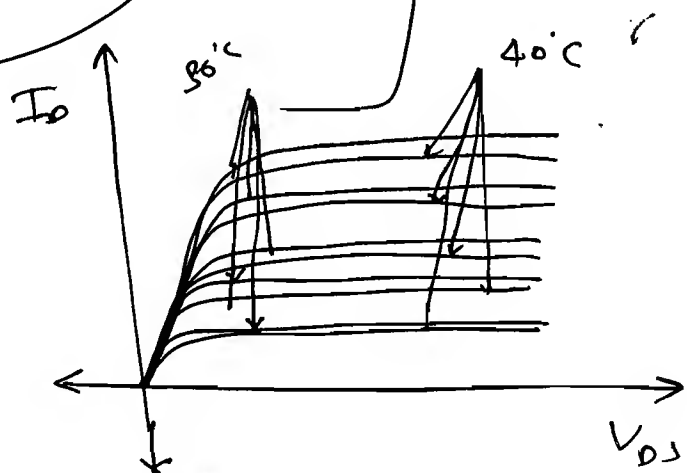
$$\mu_n \propto \frac{1}{T^m} \Rightarrow \mu \propto T^{-m}.$$

$$T \uparrow \rightarrow \mu_n \downarrow \rightarrow I_D \downarrow$$

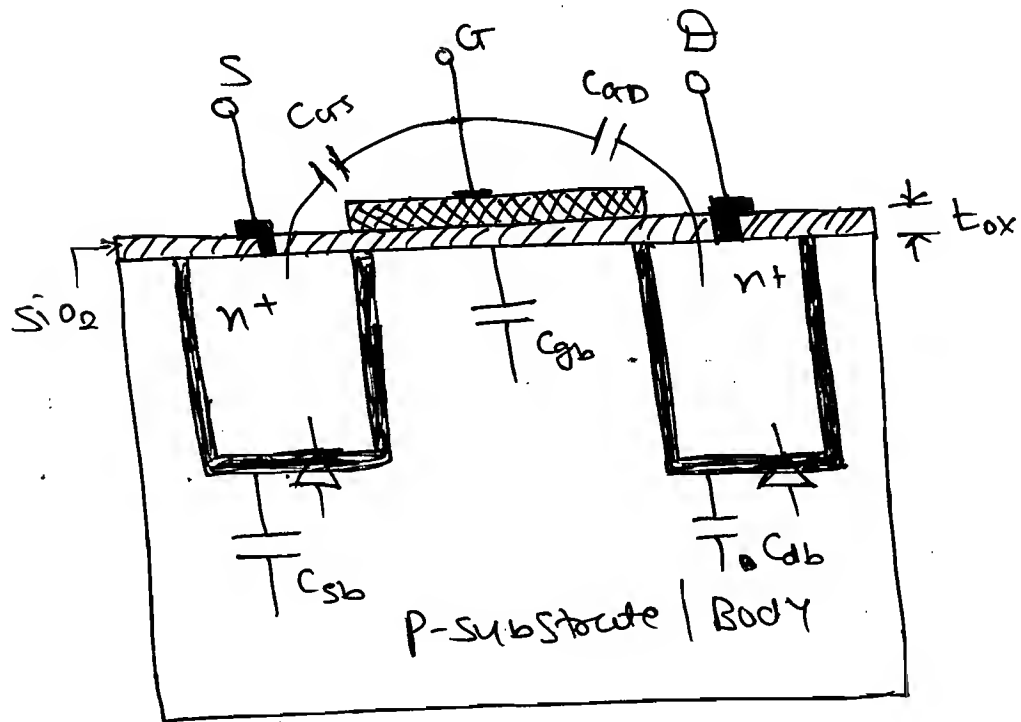
NTC

$$T \uparrow \rightarrow I_D \downarrow$$

NTC



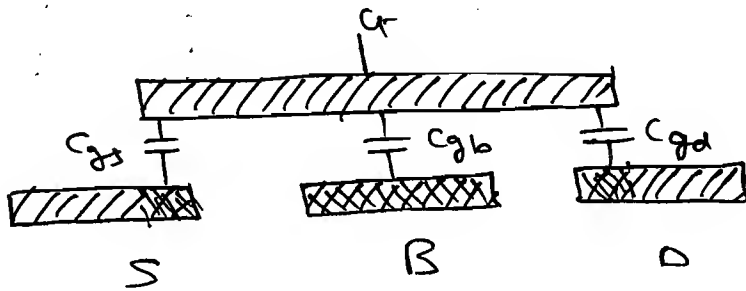
# \* Mos Capacitors: (Imp):



## ① Gate Capacitors:

- (i) Gate to Source  $C_{gp}$  ( $C_{gs}$ )
- (ii) Gate to drain  $C_{gp}$  ( $C_{gd}$ )
- (iii) Gate to body  $C_{gp}$  ( $C_{gb}$ )

⇒



$$C_g = C_{gs} + C_{gd} + C_{gb}$$

$C_g$ : Total gate capacitance.

## ② Junction Capacitors:

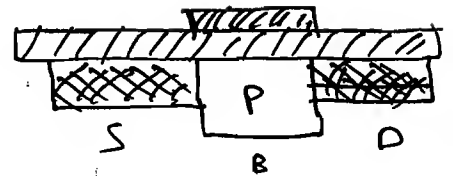
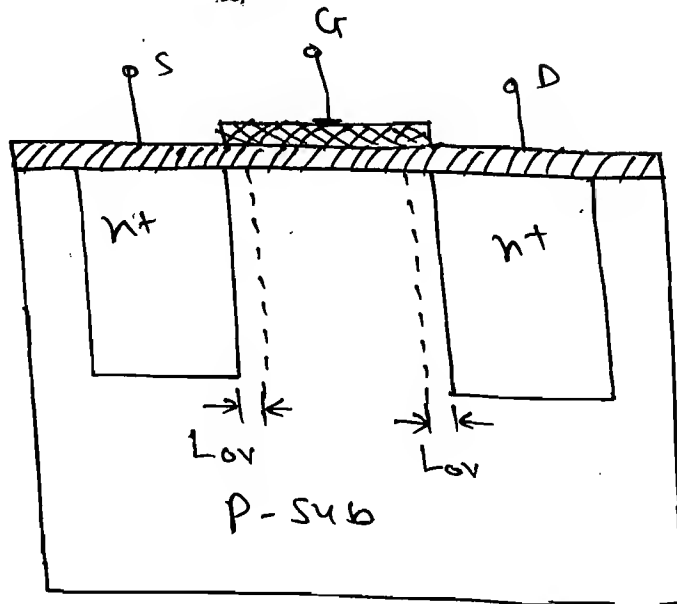
- (i) Source to body junction  $C_{jp}$  ( $C_{sb}$ )
- (ii) Drain to Body junction  $C_{jp}$  ( $C_{db}$ )

# 1. Gate Capacitors:

$$\rightarrow C_{gs} = 0 + C_{ox} \cdot W L_{ov} \quad * \quad \underline{\underline{Cut-off}}$$

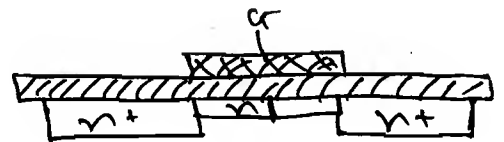
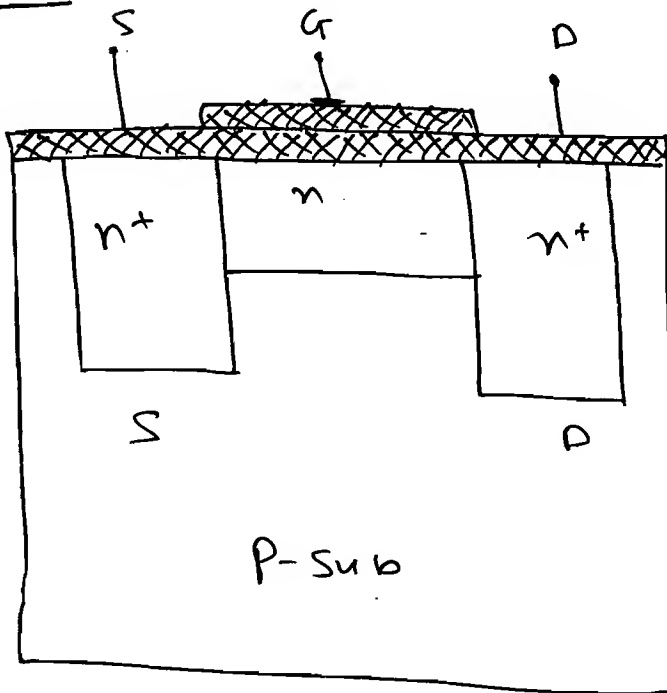
$$C_{gd} = 0 + C_{ox} \cdot W L_{ov}$$

$$C_{gb} = C_{ox} \cdot W L$$



$$C_0 = C_{ox} \times W L$$

## \* Linear:



$$C_{gs} = \frac{1}{2} C_{ox} \cdot W L + C_{ox} W L_{ov}$$

$$C_{gd} = \frac{1}{2} C_{ox} W L + C_{ox} \cdot W L_{ov}$$

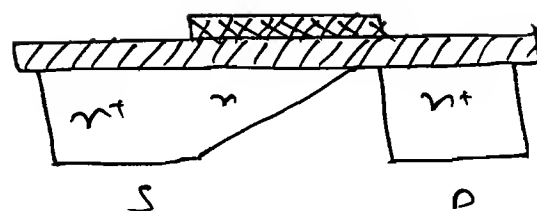
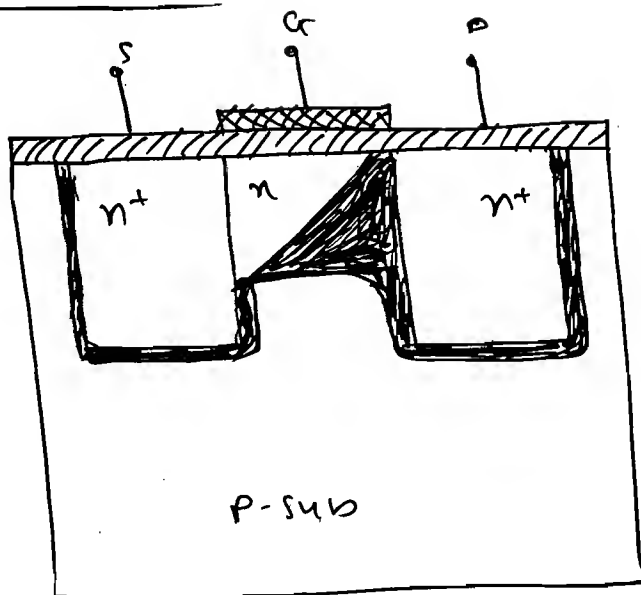
$$L_{eff} = L - 2 \Delta L_{ov}$$

$$C_{gb} = 0 \quad \text{Here, } L \text{ is by default eff. length}$$



# \* Saturation:

61)



$$\Rightarrow C_{gs} = \frac{2}{3} C_{ox} W L + C_{ox} \cdot W L_{ov}$$

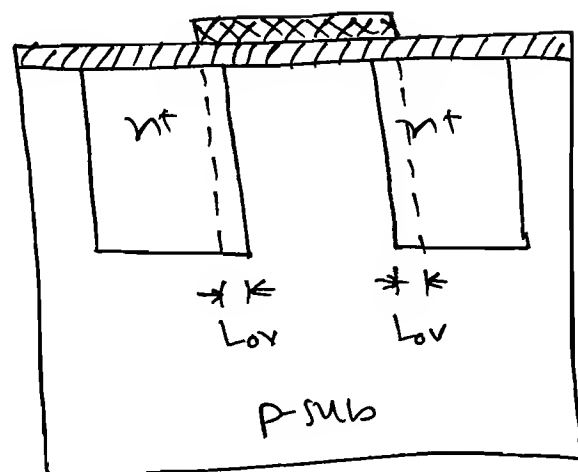
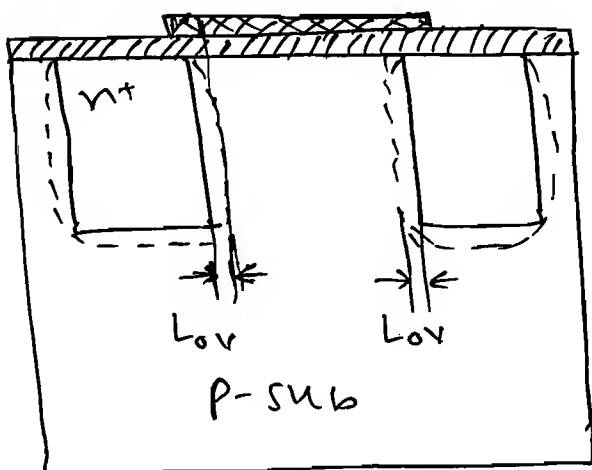
$$C_{gd} = C_{ox} \cdot W L_{ov}$$

$$C_{gb} = 0$$

$\Rightarrow$

$C_{ij}$	Cut off	Linear	Saturation
$C_{gs}$	0	$\frac{1}{2} C_0$	$\frac{2}{3} C_0$
$C_{gd}$	0	$\frac{1}{2} C_0$	0
$C_{gb}$	$C_0$	0	0
$C_g$	$C_0$	$C_0$	$\frac{2}{3} C_0$

## \* $L_{ov}$ : overlap Length:



$$C_{ov} = C_{ox} W L_{ov}$$

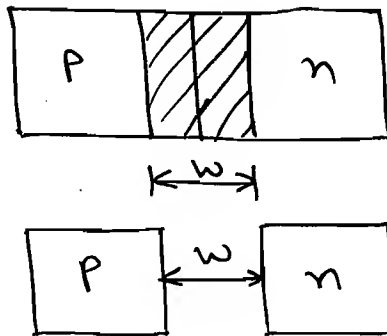
## 2. Junction Capacitors:

~~junction~~ ~~capacitor~~ ~~junction~~ ~~capacitor~~

⇒ It is also called (or) Space Charge

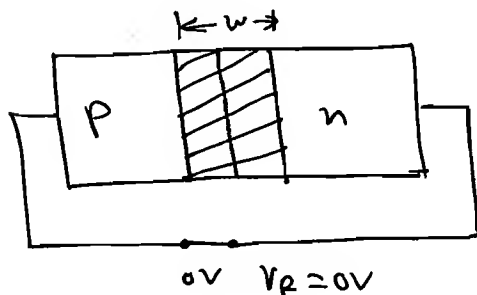
as Depletion Capacitance Capacitance.

①



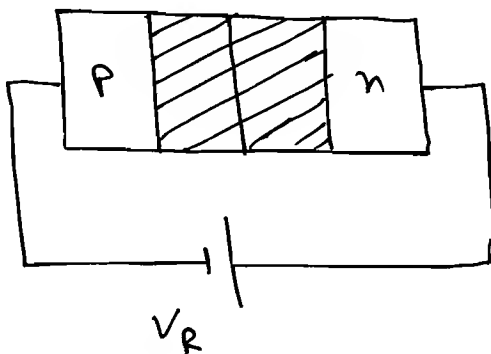
$$C_T = \frac{\epsilon A}{w}$$

②



$$C_{T0} = \frac{\epsilon A}{w}$$

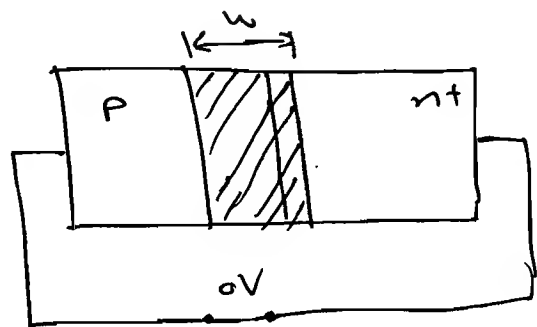
③



$$C_T = \frac{C_{T0}}{\left[1 + \frac{V_R}{V_0}\right]^{1/3}}$$

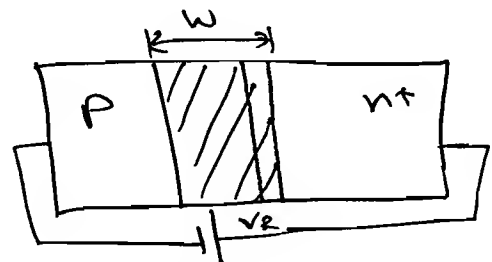
$$C_{j0} = \frac{C_{j0}}{\left[1 + \frac{V_R}{V_0}\right]^{1/3}}$$

①



$$C_{T0} = \frac{\epsilon A}{w} ; C_{j0} = \frac{\epsilon A}{w}$$

②

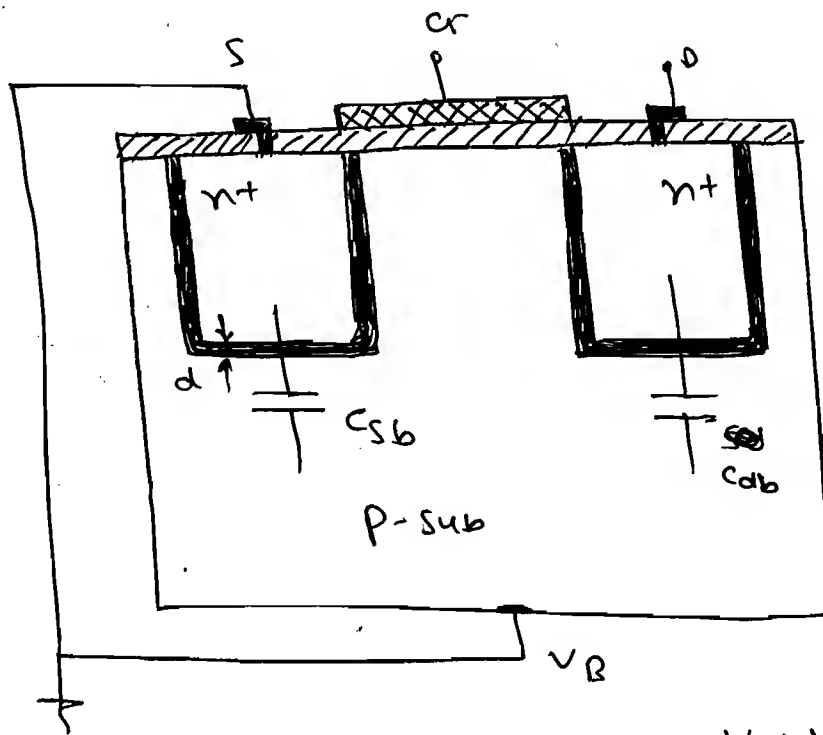


$$C_j = \frac{C_{T0}}{\left[1 + \frac{V_R}{V_0}\right]^{1/2}}$$

$$C_j = \frac{C_{j0}}{\left[1 + \frac{V_R}{V_0}\right]^{1/2}}$$

# (i) Source to Body Junction Capacitance:-

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⇒  $V_{SB}$ : Source to body Voltage.

$$C_{sbo} = \frac{\epsilon_{si} A}{d}$$

$C_{sbo}$ : Source to Body Junction when

$$V_{SB} = 0V$$

$A$ : Common area b/w Source and Body.

$d$ : depletion layer thickness b/w Source and Body.

$\epsilon_{si}$ : permittivity of Si

$$\epsilon_{si} = \epsilon_{ssi} \cdot \epsilon_0, \quad \epsilon_{ssi} = 11.7 \approx 12.$$

$$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m.}$$

$$\Rightarrow C_{sb} = \frac{C_{sbo}}{\left[1 + \frac{V_R}{V_0}\right]^{1/2}}$$

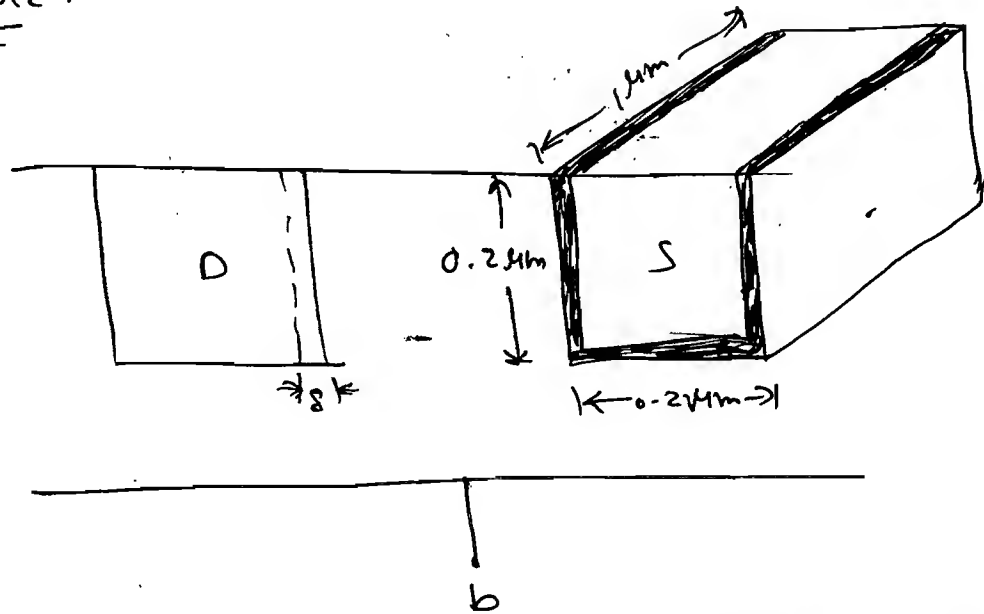
$$\therefore C_{sb} = \frac{C_{sbo}}{\sqrt{1 + \frac{V_R}{V_0}}}$$

$C_{sb}$ : Source to body Capacitance at a given  $V_{SB}$ .  
 $V_0$ : Built in potential (or) contact potential.

Q Gate-2012:

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Q-8



Obs

⇒ In 3-dimension there are three sides at which p-n junction is created. (i) bottom (ii) Left (iii) Right. So, we should consider total area bet<sup>n</sup> body and source for  $C_{sb}$  calculation.

∴ and here no biasing is provided

$$\therefore C_{sb} = C_{sbo} = \frac{\epsilon_{si} \cdot A}{d}$$

$$\therefore A = (0.2 \mu \times 0.2 \mu) + (0.2 \times 1 \mu) + (0.2 \mu \times 1 \mu)$$

$$= 3 \times 0.2 \times 10^{-6} \times 1 \times 10^{-6}$$

$$\therefore A = 0.6 \times 10^{-12} \text{ m}^2$$

$$\therefore C_{sb} = \frac{11.7 \times 8.9 \times 10^{-12} \times 0.6 \times 10^{-12}}{10 \times 10^{-9}}$$

$$\therefore C_{sb} = 6.24 \times 10^{-15}$$

$$\therefore C_{sb} = 6.24 \text{ fF} \approx 7 \text{ fF}$$

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if we consider front and back area  
then

$$A = (3 \times 0.2 \times 10^{-12}) + (2 \times 0.2 \times 0.2 \times 10^{-12})$$

$$A = 0.68 \times 10^{-12} \text{ m}^2$$

2

$$C_{sb} = 7.024 \text{ fF}$$

Q-9

Soln:

$$C_{gs_{ov}} = \frac{\epsilon_{si} \epsilon_0 W L_{ov}}{d}$$

$$C_{gs_{ov}} = \frac{3.9 \times 8.9 \times 10^{-12} \times 10^{-6} \times 20 \times 10^{-9}}{10 \times 10^{-9}}$$

$$\therefore C_{gs_{ov}} = 0.7 \text{ fF.}$$

2. Drain to Body j<sub>n</sub> Capacitor:

$\Rightarrow V_{dB} =$  Drain to Body Voltage.

$$C_{db0} = \frac{\epsilon_{si} A}{d}$$

$C_{db0} =$  drain to body capacitance when  $V_{SB} = 0$ .

$d$ : depletion layer thickness bet<sup>n</sup> D & S.

$A$ : Common area bet<sup>n</sup> D & S.

$\epsilon_{si}$ : permittivity of Si

$$\epsilon_{si} = \epsilon_{si} \cdot \epsilon_0, \quad \epsilon_{ssi} = 11.7 \approx 12.$$

$$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m.}$$

⇒

$$C_{db} = \frac{C_{dso}}{\sqrt{1 + \frac{V_{db}}{V_0}}}$$

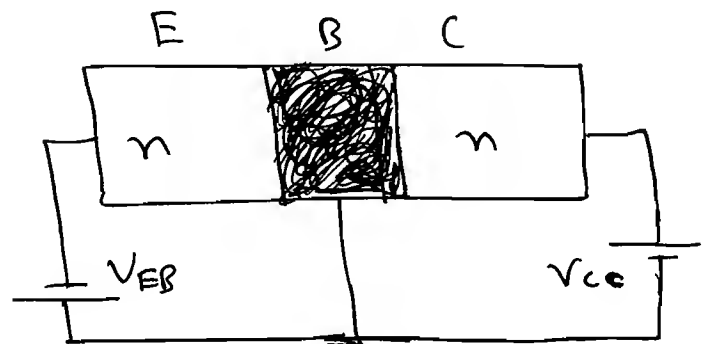
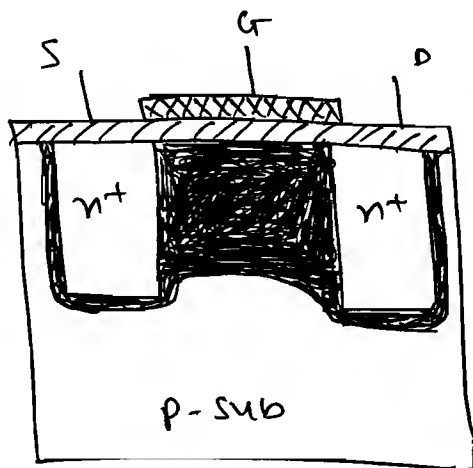
$C_{db}$  : Drain to body Capacitor wh- at a given  $V_{gs}$ .

$V_0$  : Built in Potential at Constant Potential.

\* Short Channel effect :-

1. Punch through:

⇒

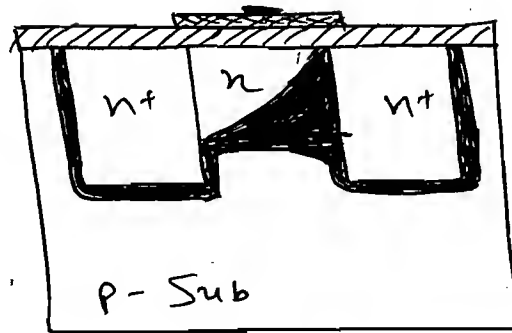


⇒ For Short Channel MOSFET in the Saturation region as drain to source Voltage increases. The width of the drain depletion region increases. At a particular value of  $V_{ds}$ , drain depletion region penetrates through channel to the source. It is called Punch through (or) Reach-through.

## 2. Avalanche Break Down:

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⇒



⇒ As drain to source voltage increases, the width of the drain depletion region increases. At a particular value of  $V_{DS}$ , this depletion region gets breakdown due to avalanche effect. Therefore, it is called avalanche effect.

⇒ Due to punch through effect (or) avalanche breakdown, the MOSFET never gets damage.

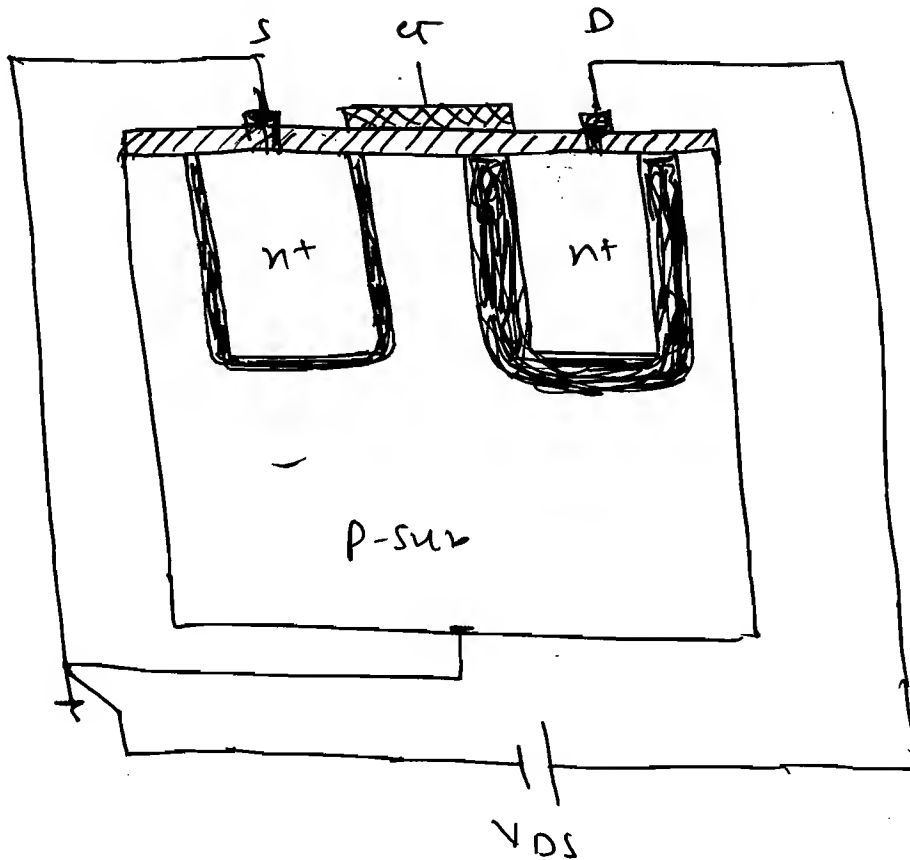
## 3. Gate-oxide Break-Down:

⇒ As gate to source voltage increases at a particular value of  $V_{GS}$ , the oxide layer bet<sup>n</sup> gate and source gets damage (or) breakdown it is called gate-oxide breakdown.

⇒ Gate oxide B-D is a permanent damage to the MOSFET.

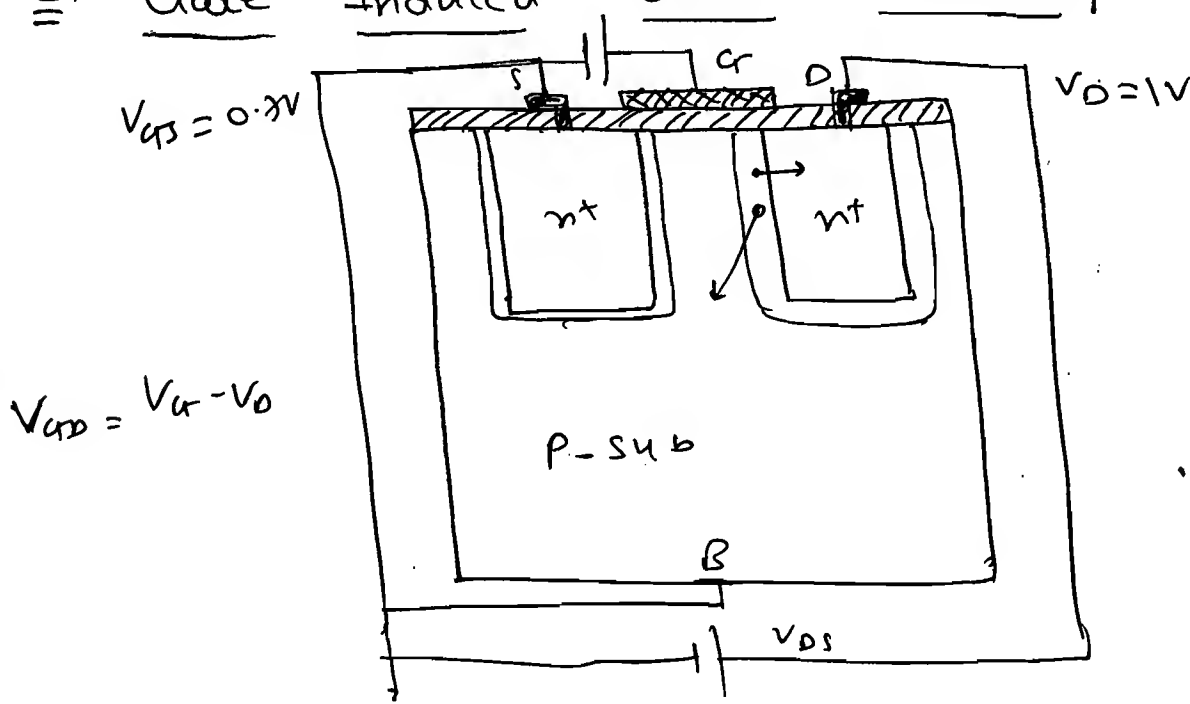
#### 4. Drain Included Barrier Lowering (DIBL):

⇒

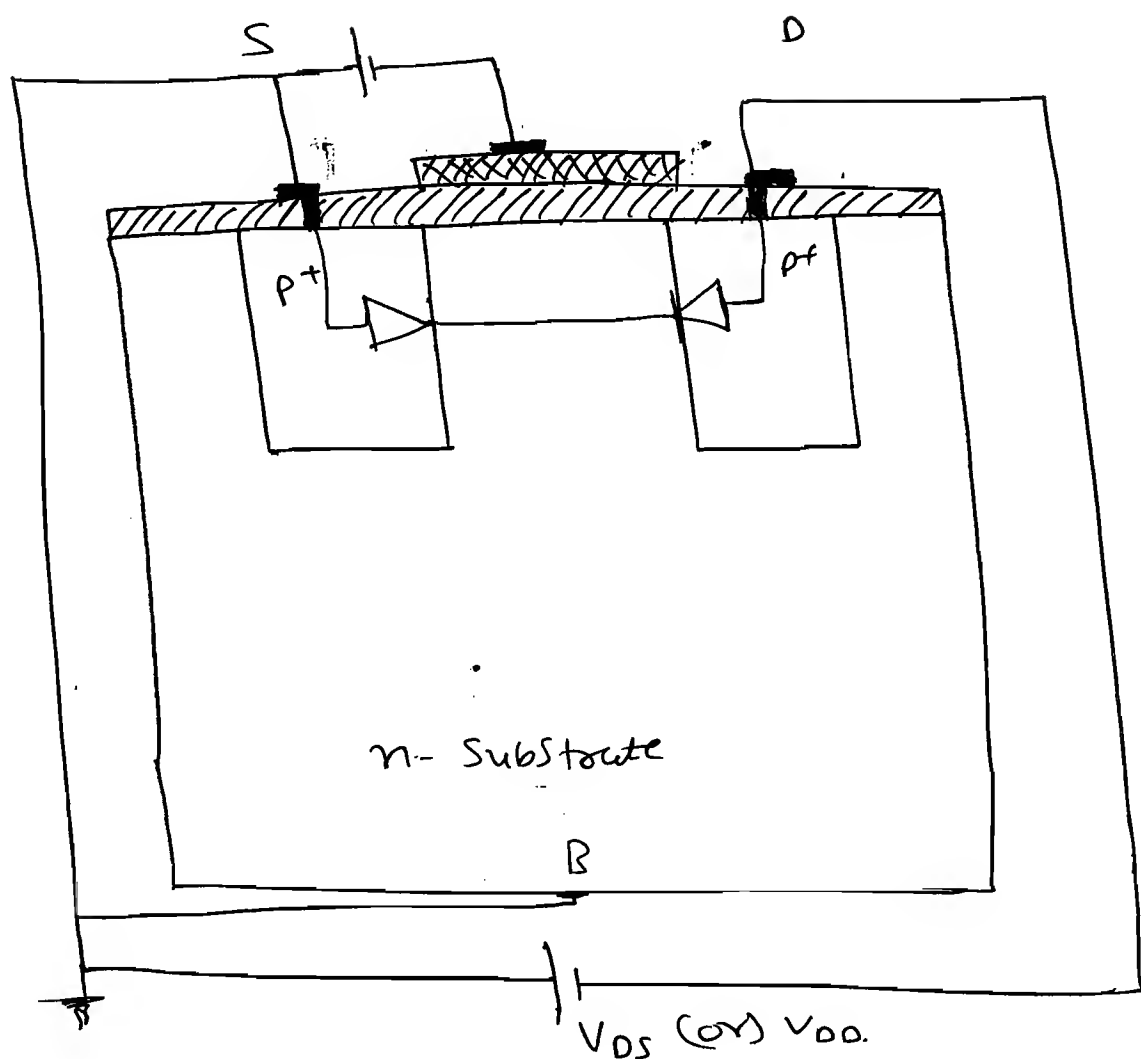


⇒ As drain to source voltage increases, the width of the drain depletion region increases. Therefore, threshold voltage decreases. i.e. it forms a channel for lower value of  $V_{GS}$ .

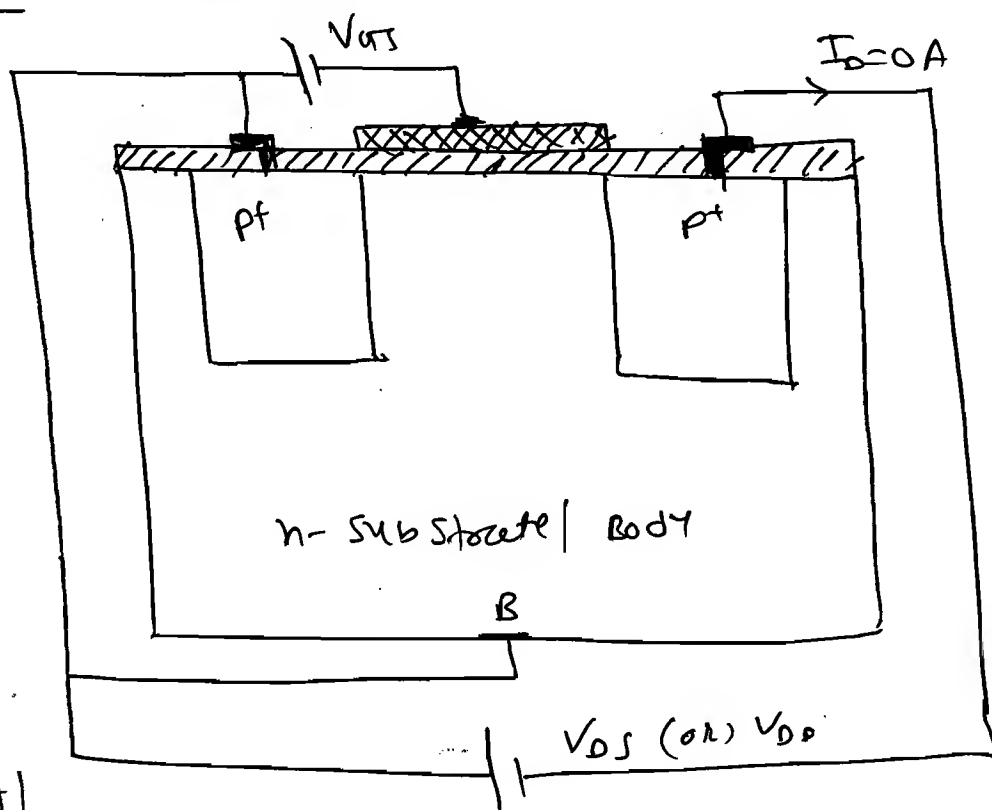
#### 5. Gate Induced drain Leakage (GIDL):





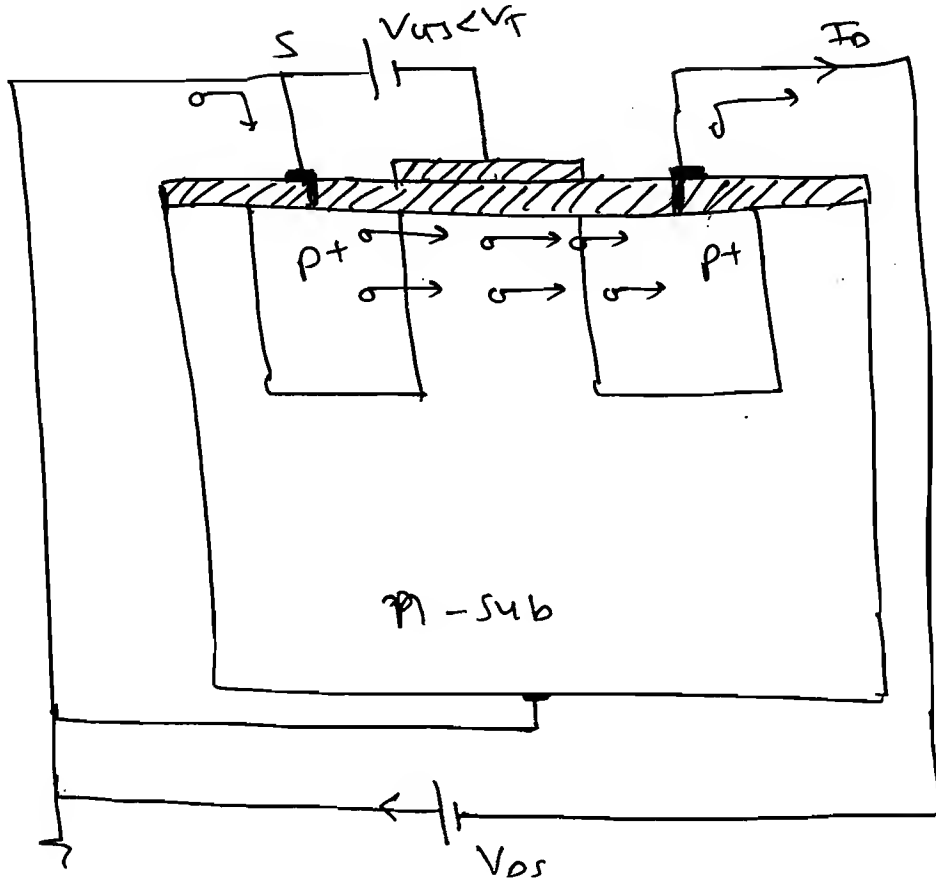


①  $V_{GS} > V_T$  : Cut-off:



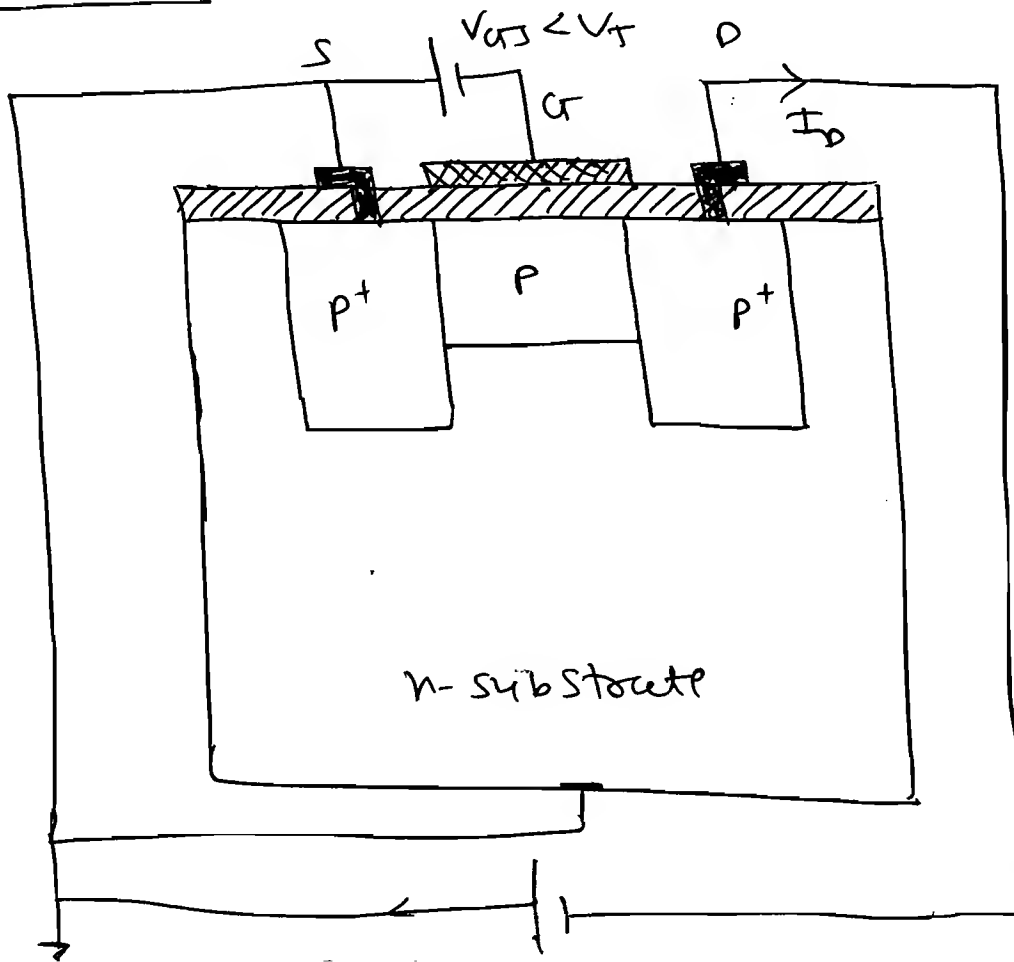
$$|V_{rs}| < |V_T|$$

②  $V_{GS} < V_T$  &  $V_{DS} > V_{GS} - V_T$  : Linear.



$|V_{GS}| > |V_T|$  &  $|V_{DS}| < |V_{GS} - V_T|$ .

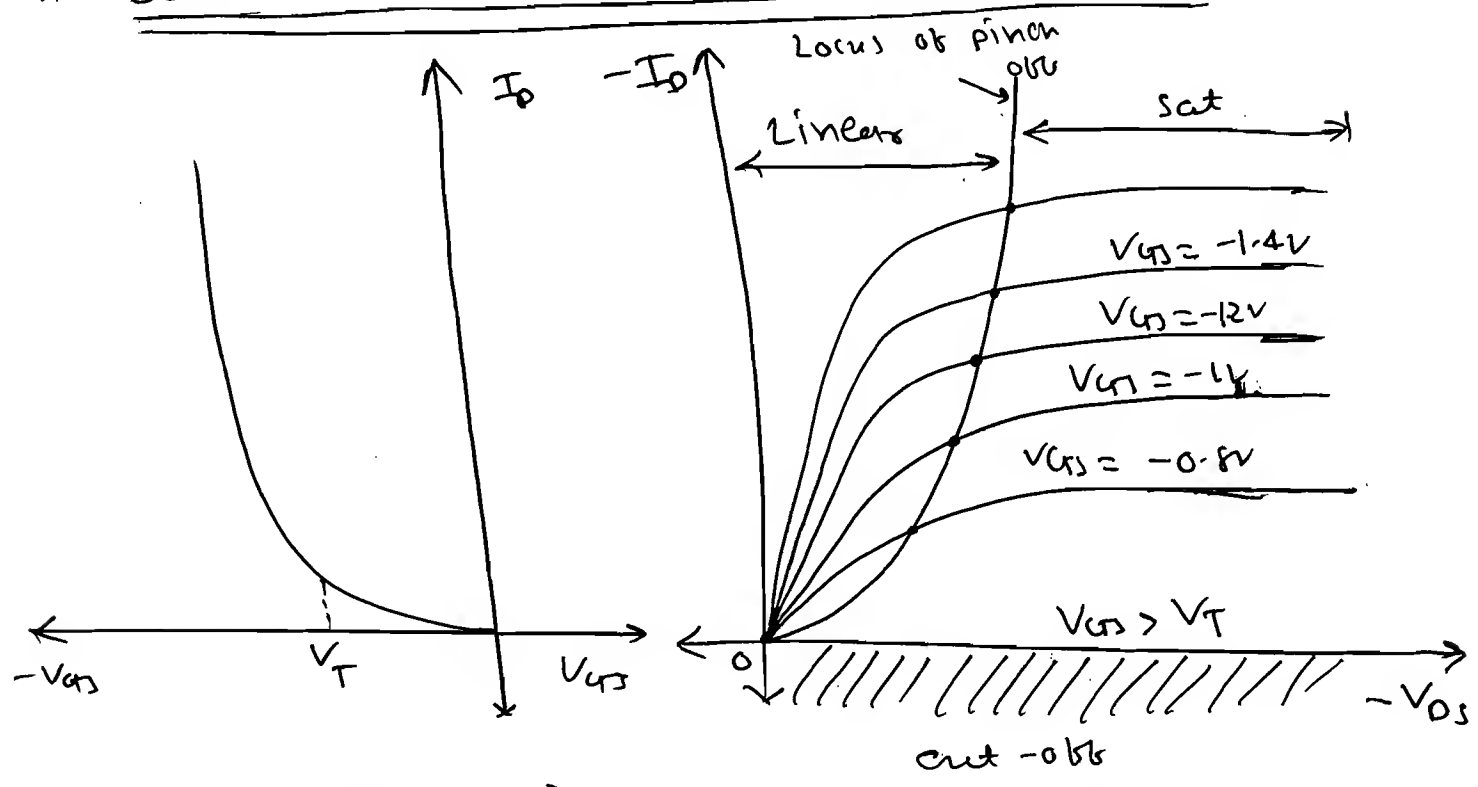
③  $V_{GS} < V_T$  &  $V_{DS} < V_{GS} - V_T$  : Saturation.



$$\Rightarrow |V_{GS}| < |V_T| \text{ \& } |V_{DS}| > |V_{GS} - V_T|$$

$$V_{DS} = -V_E, \quad V_{GS} = -V_E, \quad V_T = -V_E$$

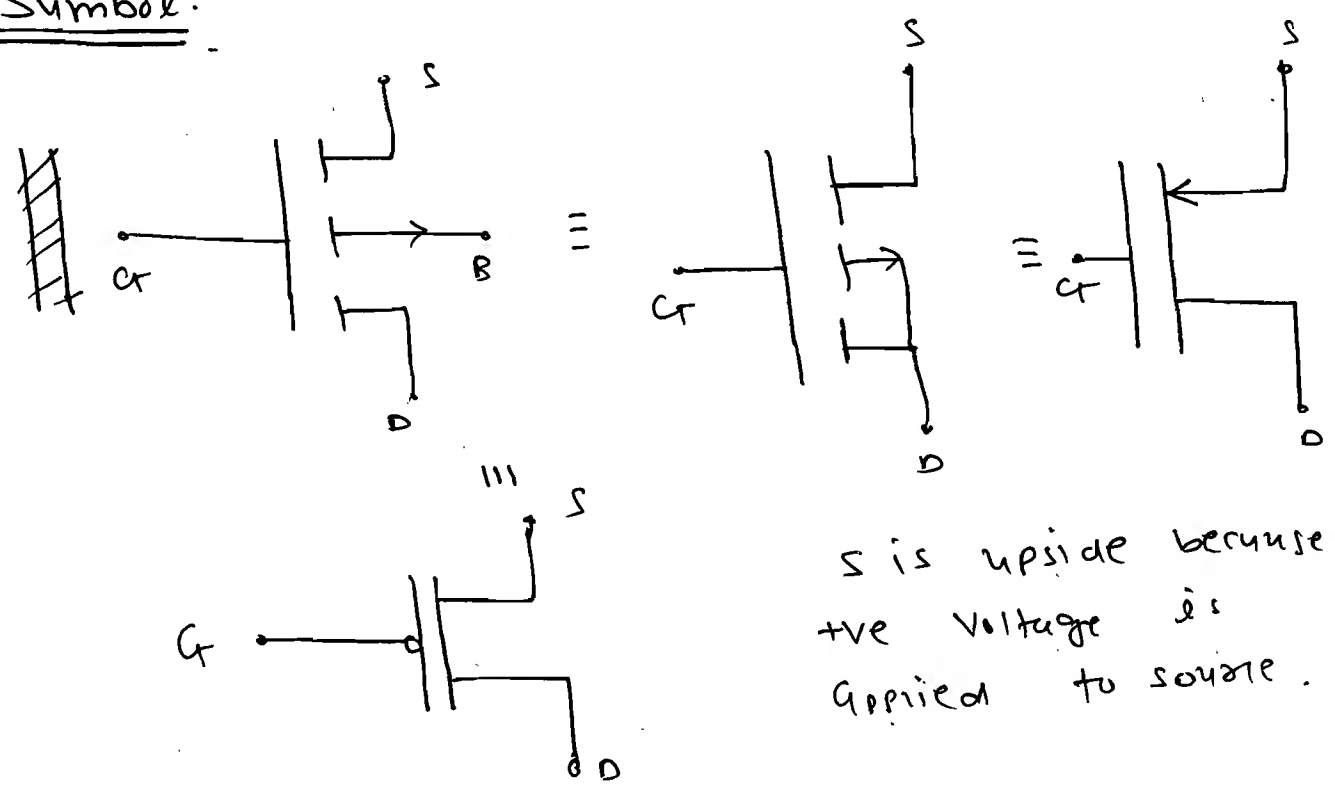
# \* Drain and Transfer Characteristics



## Transfer Characteristics

## Drain Characteristics

### \* Symbol:



S is upside because +ve voltage is applied to source.

\* Condition for pinch-off:

$$\Rightarrow V_{DS} = V_{GS} - V_P$$

$\uparrow$                        $\uparrow$                        $\uparrow$   
 -ve                      -ve                      -ve

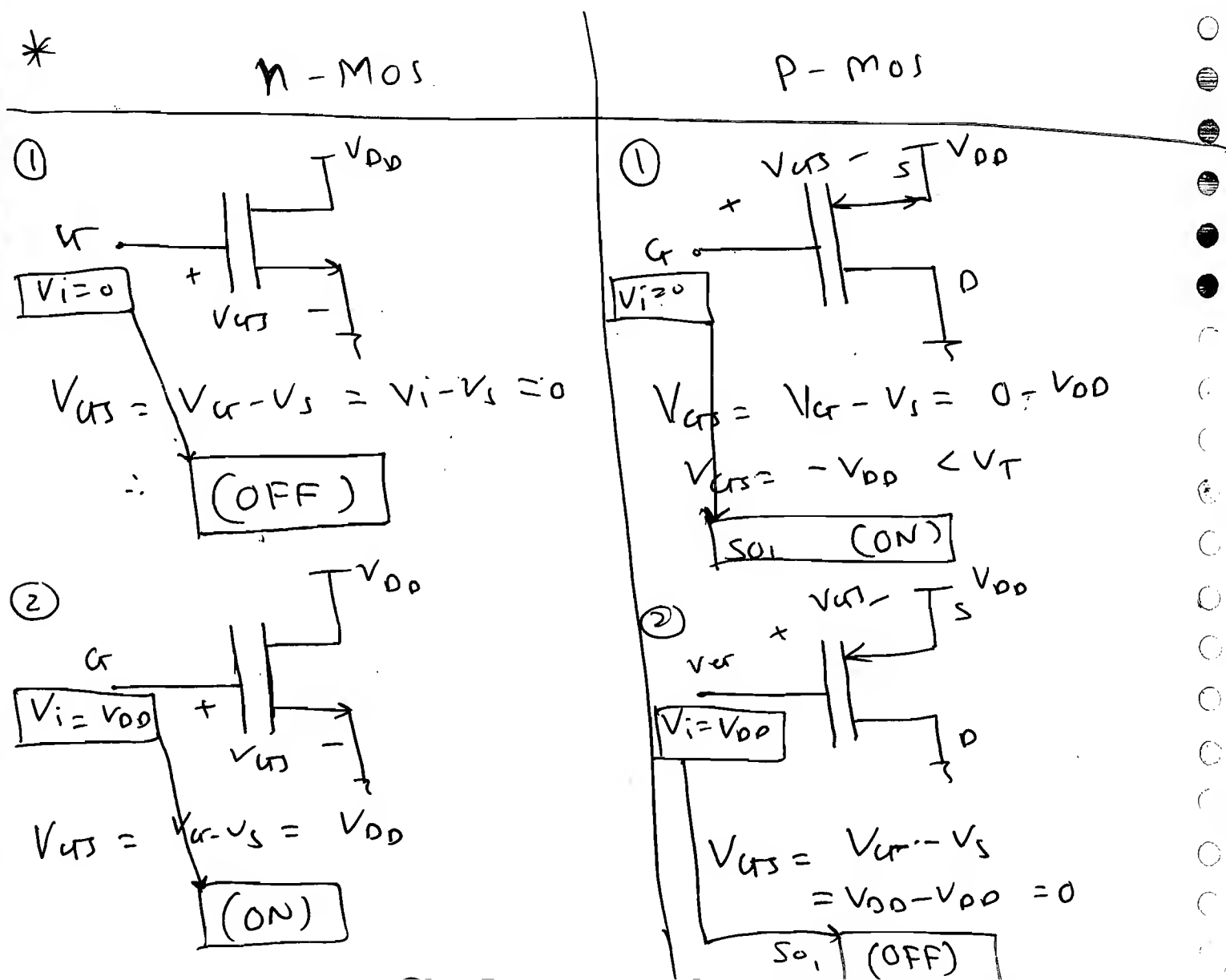
$$\Rightarrow V_{DS} > V_{GS} - V_P : \text{Linear}$$

$$V_{DS} < V_{GS} - V_P : \text{Sat.}$$

\*

	n-MOS	p-MOS
$V_{GS} = 0$	OFF	OFF
$V_{GS} = +ve$ i.e. ( $V_{GS} > V_T$ ):	ON	OFF
$V_{GS} = -ve$ i.e. ( $V_{GS} < V_T$ ):	OFF	ON

\*



## \* Imp Points to be remember:

$\Rightarrow$  P-Channel MOSFET operates with -ve gate voltages i.e. -ve  $V_{GS}$  values.

$\Rightarrow$  Gate-to-source Voltage (i.e.  $V_{GS}$ ) and Threshold Voltage ( $V_T$ ) are -ve for p-channel enhancement MOSFET.

$\Rightarrow$  P-Channel E-MOSFET operates in enhancement mode for -ve  $V_{GS}$  values.

$\Rightarrow$  In discrete P-EMOSFET, substrate (or) Body (or) Bulk is connected to source terminal (or)  $V_{DD}$ . Whereas in ICs it should be connected to most +ve values.

$\Rightarrow$  P-EMOSFET will be on for -ve  $V_{GS}$  values (i.e.  $V_{GS} < V_T$ ) and it will be OFF for 0 or +ve  $V_{GS}$  values i.e. ( $V_{GS} > V_T$ )

$\Rightarrow$  Condition for pinch-off (or) saturation is  $V_{DS} = V_{GS} - V_T$ . and here, all are -ve.

$\Rightarrow$  For  $V_{GS} > V_T$  (or)  $|V_{GS}| < |V_T|$ , P-MOSFET operates in cut-off region and its drain current  $I_D = 0$ .

$\Rightarrow$  For  $V_{GS} < V_T$  and  $V_{DS} > V_{GS} - V_T$  (or)  $|V_{GS}| > |V_T|$  and  $|V_{DS}| < |V_{GS} - V_T|$

it operates in linear region and its drain current

$$I_D = \mu_p \cdot C_{ox} \cdot \frac{W}{L} \left[ \underset{\substack{\uparrow \\ -ve}}{V_{GS} - \underset{\substack{\uparrow \\ -ve}}{V_T}} V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$\mu_p$ : mobility of holes.

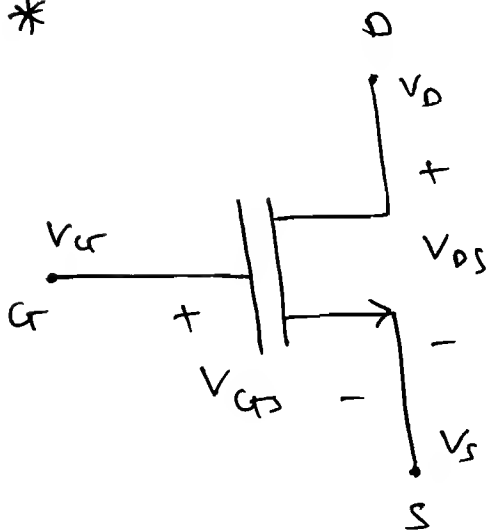
$\Rightarrow$  For  $V_{GS} < V_T$  &  $V_{DS} \leq V_{GS} - V_T$  (or)

$|V_{GS}| > |V_T|$  &  $|V_{DS}| \leq |V_{GS} - V_T|$ . it

operates in Saturation region and its drain current,

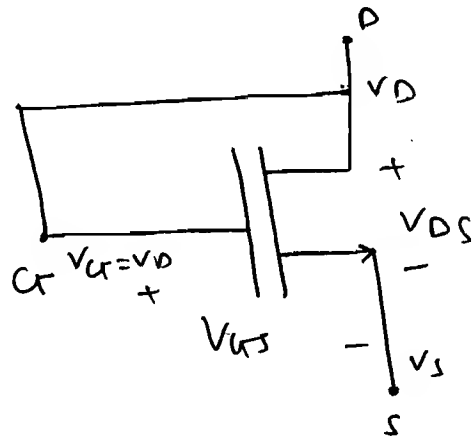
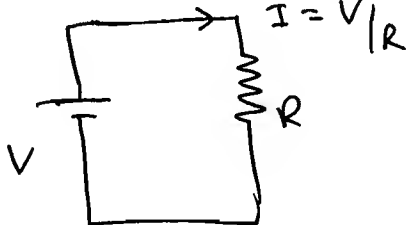
$$I_D = \frac{1}{2} \mu_p \cdot C_{ox} \cdot \frac{W}{L} [ \underset{\substack{\uparrow \\ -ve}}{V_{GS} - \underset{\substack{\uparrow \\ -ve}}{V_T}} ]^2$$

\*



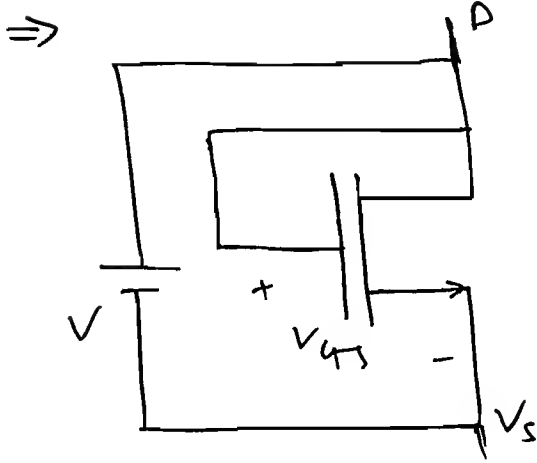
$$V_{GS} = V_G - V_S$$

$$V_{DS} = V_D - V_S$$

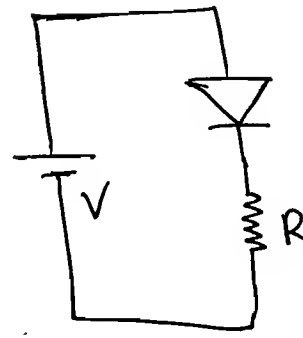


$$\rightarrow \text{if } V_G = V_D \Rightarrow V_{GS} = V_{DS}$$

$$\rightarrow \text{if } V_{GS} = V_{DS} \text{ \& } V_{GS} > V_T \Rightarrow \text{Sat}$$



$\equiv$

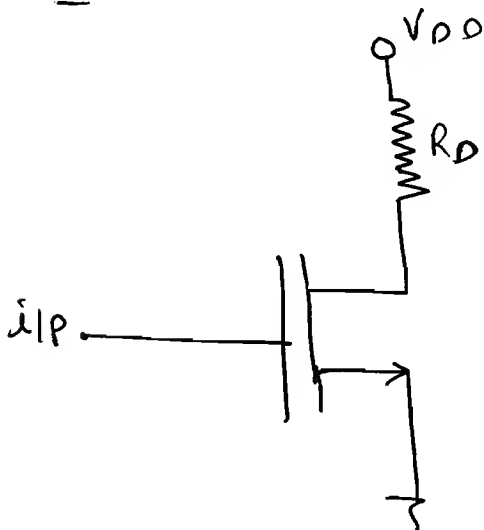


$$V_{gs} = V > V_T$$

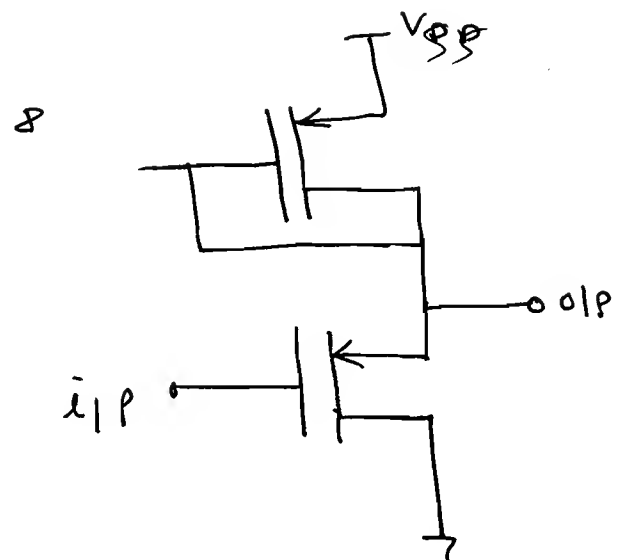
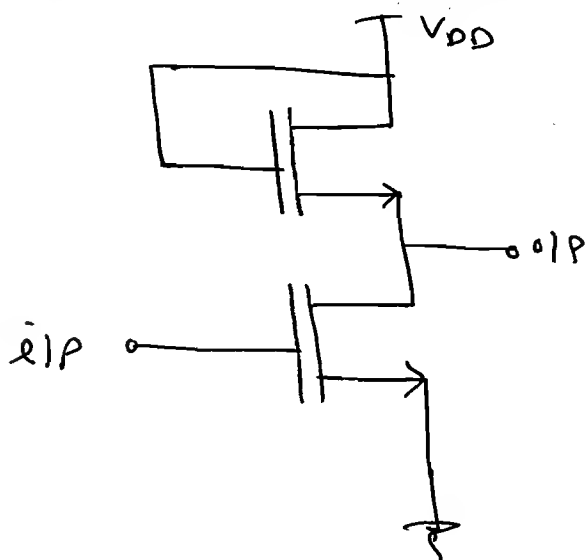
then  $I$  will flow.

### ★ Types of Load:

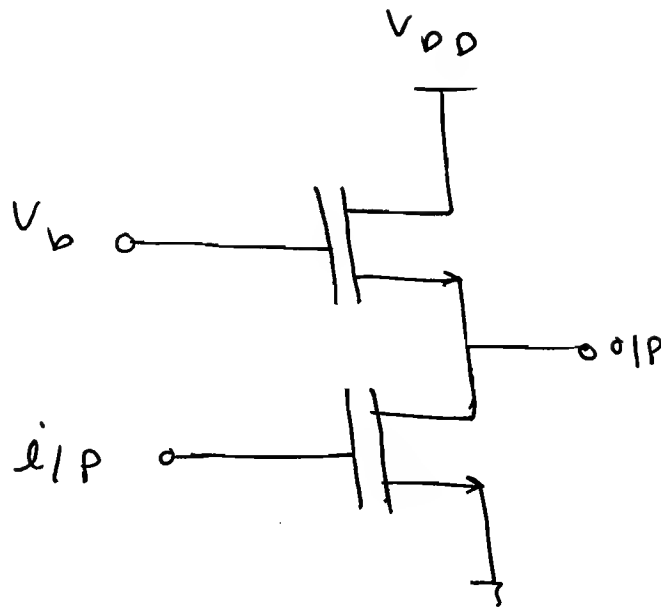
#### ① Resistive Load:



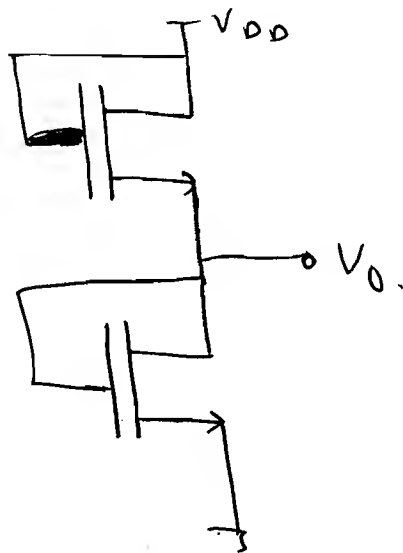
#### ② Diode connected Load:



### ③ Current - Source Load:



Q Find  $V_o$  in the given figure.



Sol<sup>n</sup>: Both are n-channel and same parameters. So, Both are ~~same~~ act as a same resistor. Hence  $V_o = \frac{V_{DD}}{2}$ .

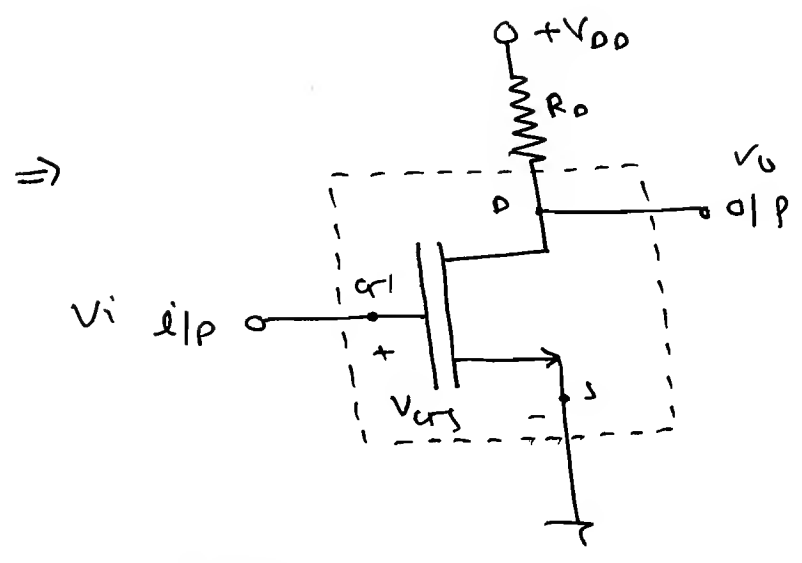
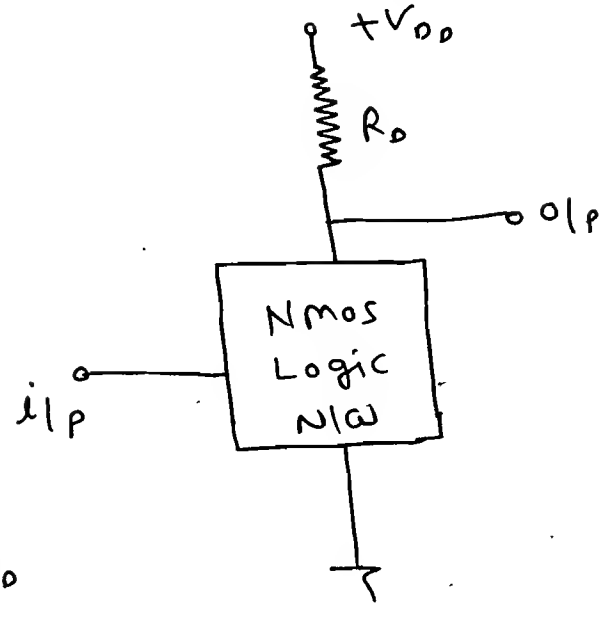


# ★ CMOS (complementary MOS):

\* n-MOS:

⇒ Inverter:

A	$\bar{A}$
0	1
1	0



(i)  $V_i = 0$

$$V_{gs} = V_g - V_s = V_i - 0$$

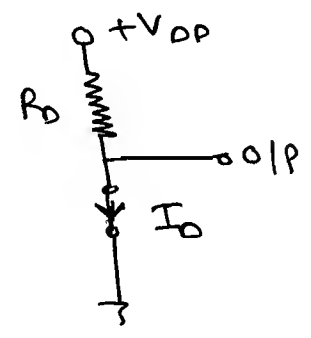
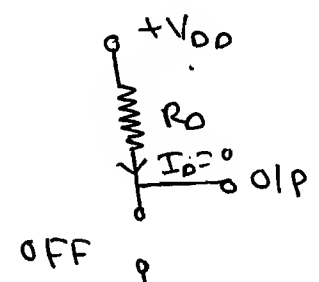
$$V_{gs} = 0$$

⇒ **OFF**

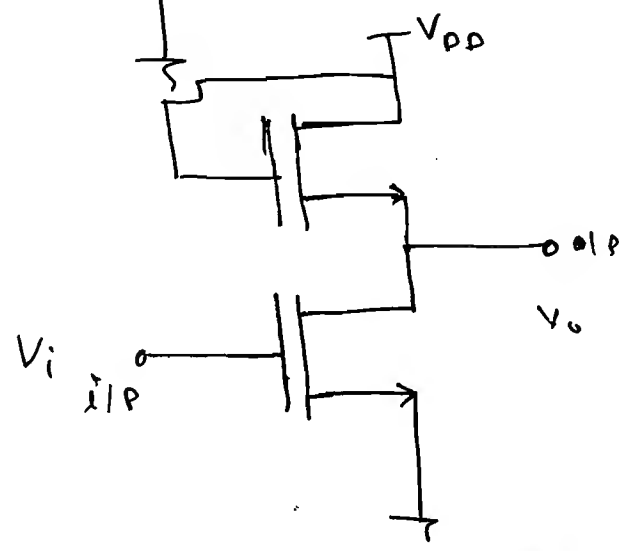
(ii)  $V_i = +V_{DD}$

$$V_{gs} = V_g - V_s = V_i - 0$$

$$V_{gs} = V_{DD} \Rightarrow \text{ON}$$

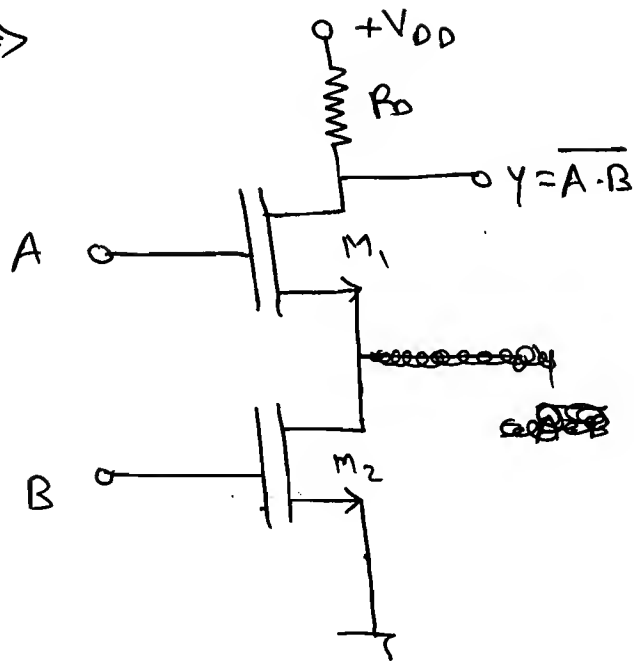


⇒



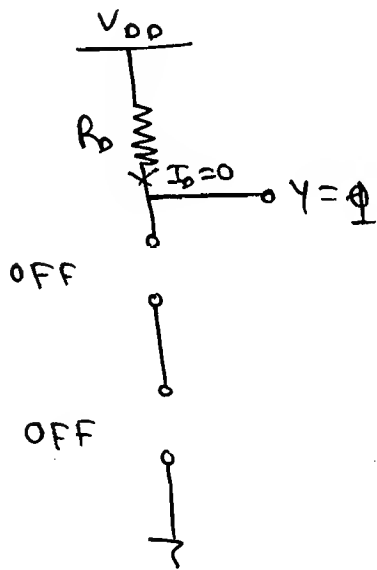
# \* 2-Input NAND Gate:-

⇒



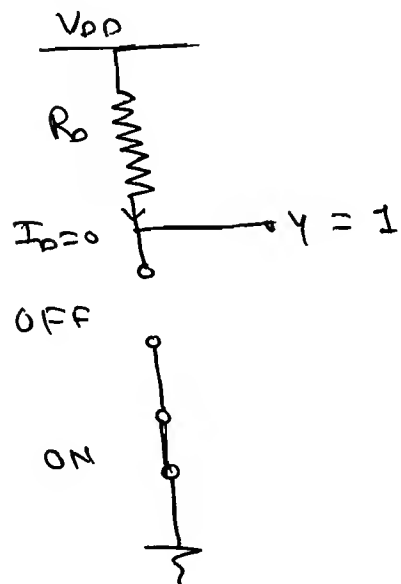
A	B	$F = A.B$
0	0	1
0	1	1
1	0	1
1	1	0

⇒ (i)  $V_i$ ,  $A=0$ ,  $B=0$ .

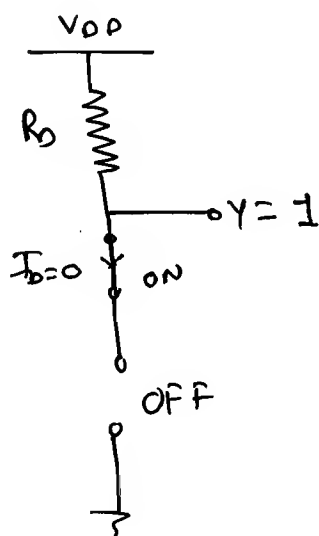


(ii)

$A=0$ ,  $B=1$ .

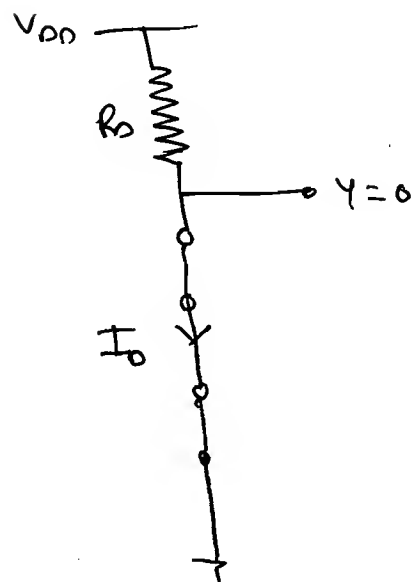


(iii)  $A=1$ ,  $B=0$



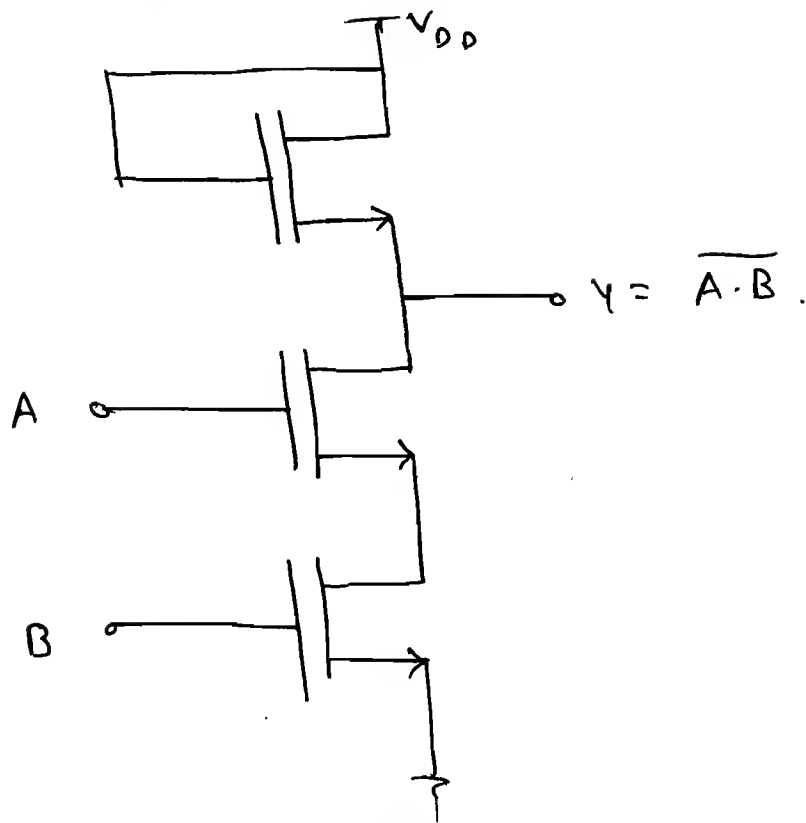
(iv)

$A=0$ ,  $B=1$



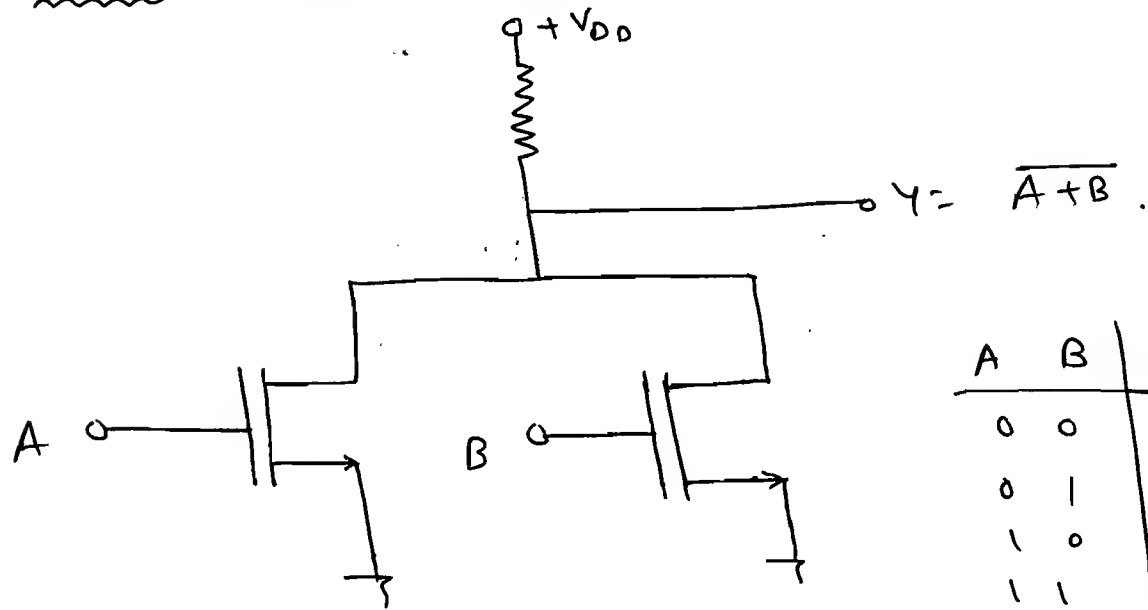
⇒ Replace  $R_D$  by one more nmos.

⇒



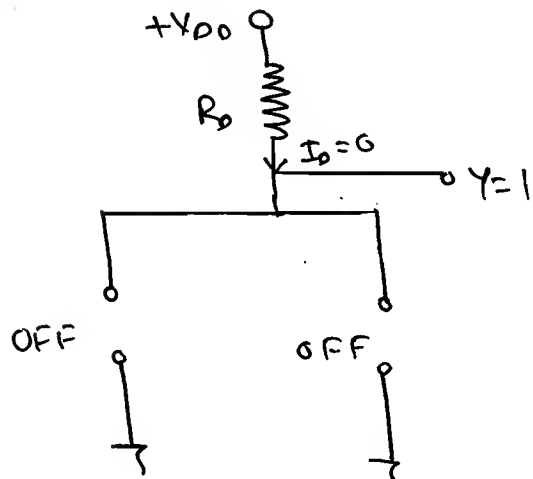
\* 2-input NOR Gate:

⇒

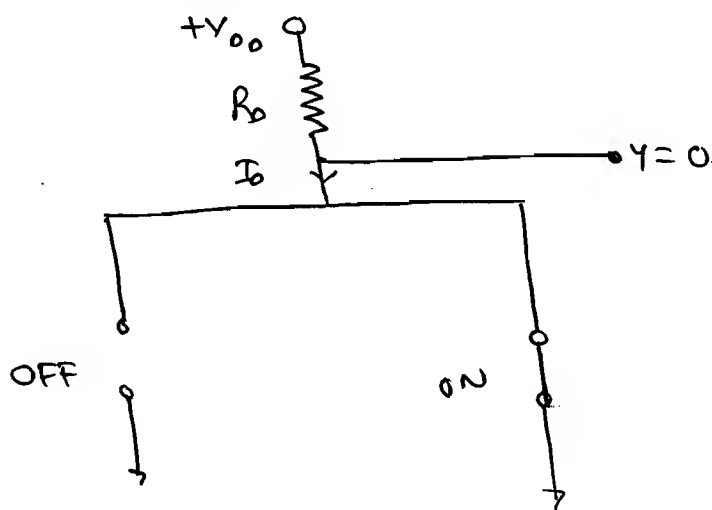


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

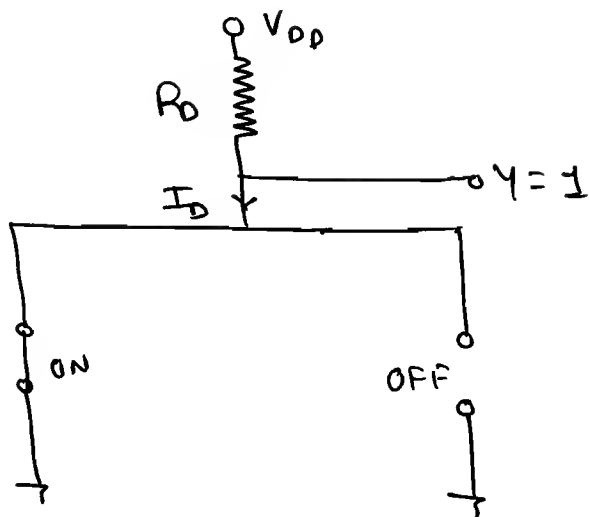
(i)  $A=0, B=0.$



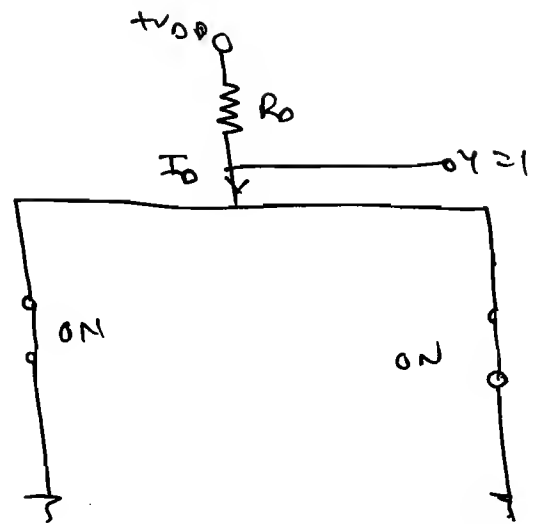
(ii)  $A=0, B=1.$



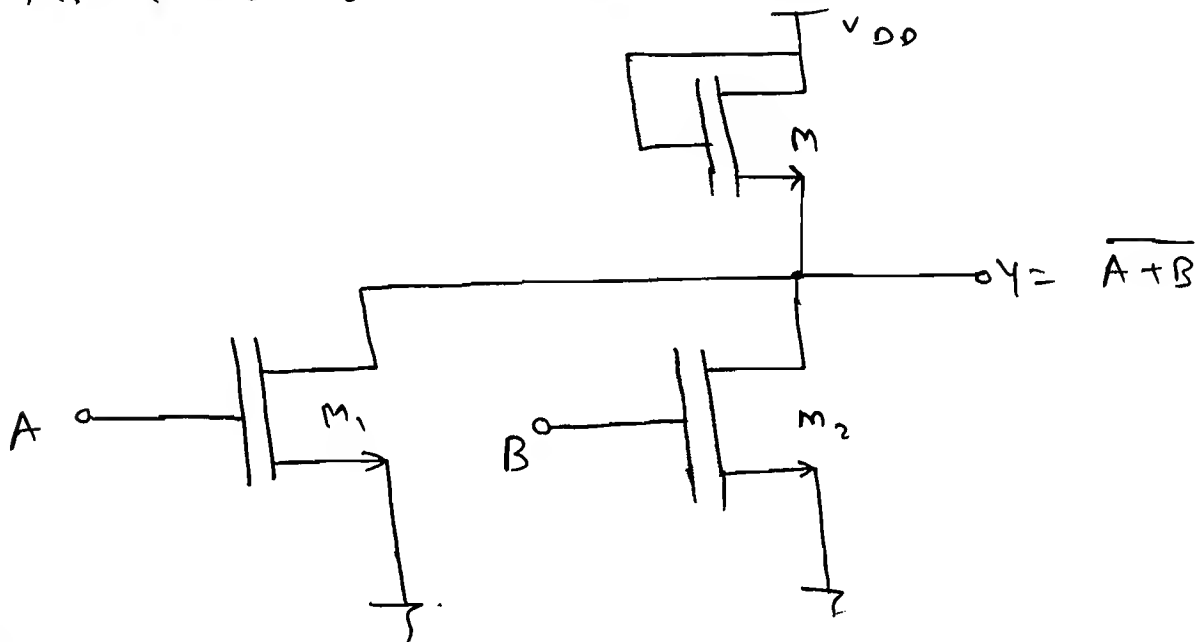
(iii)  $A=1, B=0$



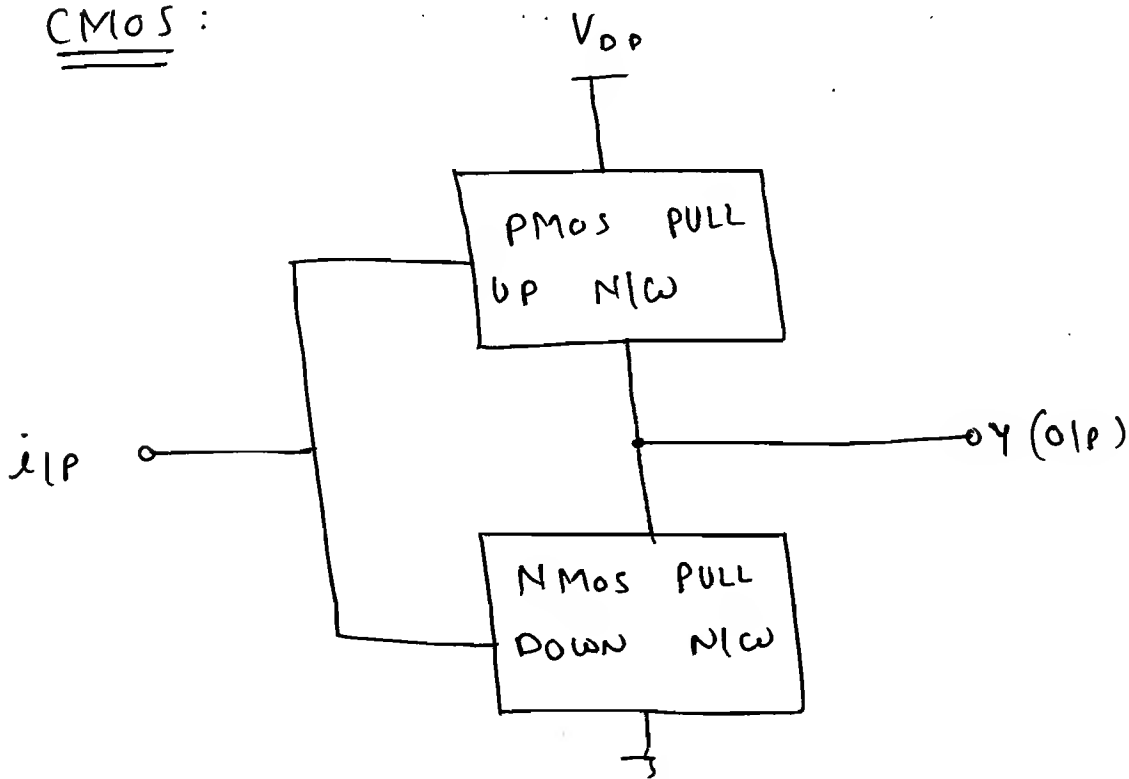
(iv)  $A=1, B=1$



$\Rightarrow$  Replace  $R_D$  by one more mos.

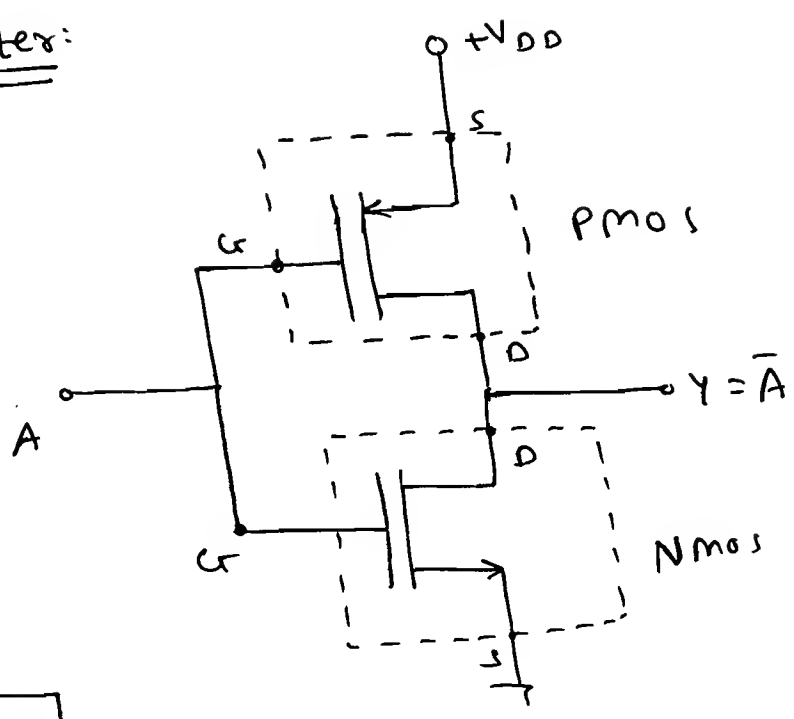


\* CMOS:



# \* Inverter:

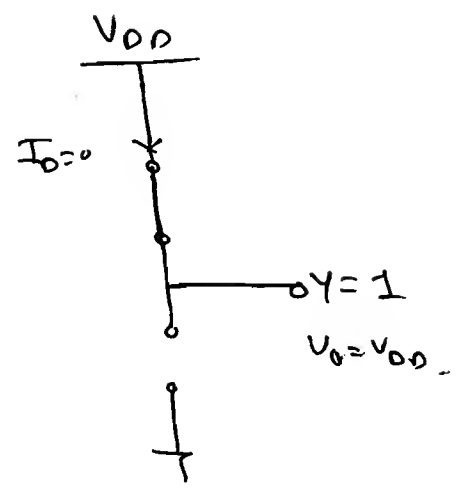
⇒



(i)  $V_i = 0$

Nmos  
 $V_{GS} = V_G - V_S$   
 $= V_i - 0$   
 $V_{GS} = V_i = 0$   
**OFF**

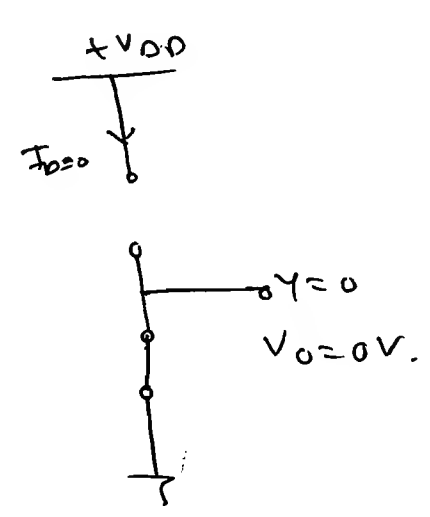
Pmos  
 $V_{GS} = V_G - V_S$   
 $= V_i - V_{DD}$   
 $V_{GS} = -V_{DD}$   
**ON**



(ii)  $V_i = +V_{DD}$

Nmos  
 $V_{GS} = V_G - V_S$   
 $= V_{DD} - 0$   
 $V_{GS} = V_{DD}$   
**ON**

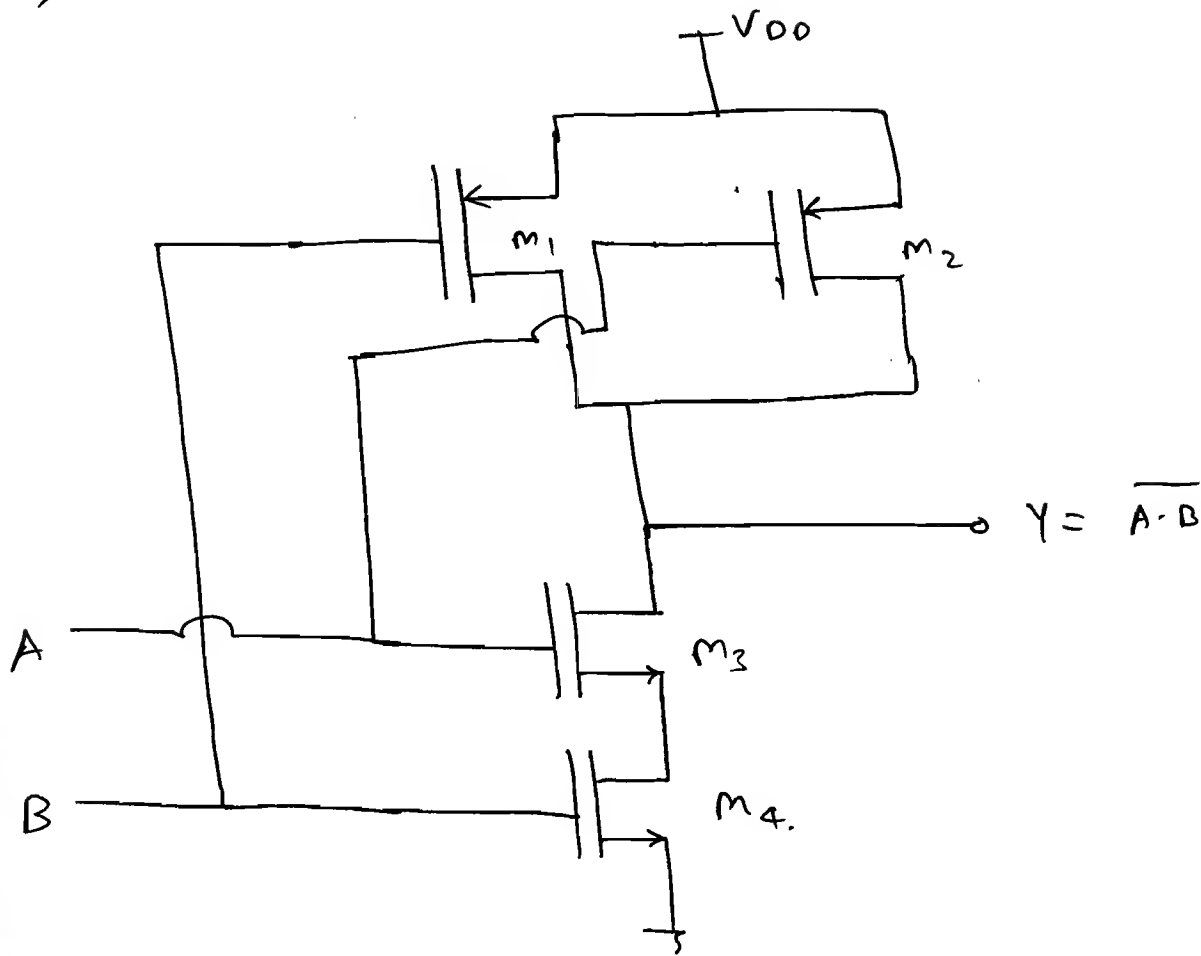
Pmos  
 $V_{GS} = V_G - V_S$   
 $= V_{DD} - V_{DD}$   
 $V_{GS} = 0$   
**OFF**



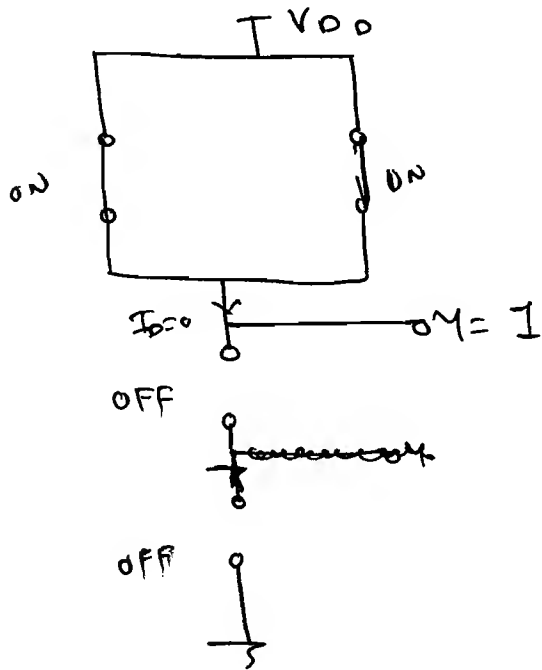
⇒ Here in both the case Ideally  $I_D$  is zero and ideally power dissipated is zero. But practically some small  $I_D$  resistance is present. So, some small power is dissipated in  $T_x$ . But it is very small compare to other technology.

\* 2 input NAND gate:

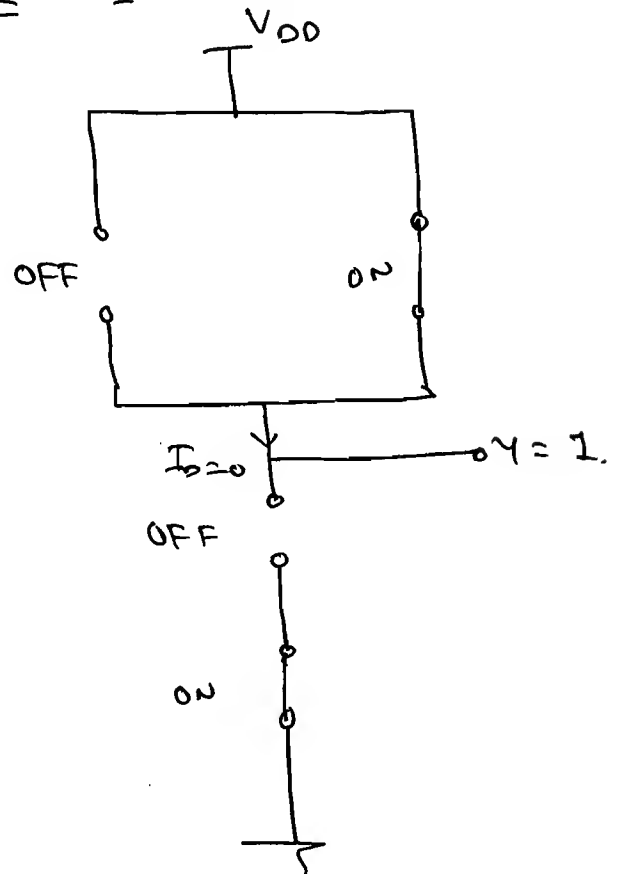
⇒



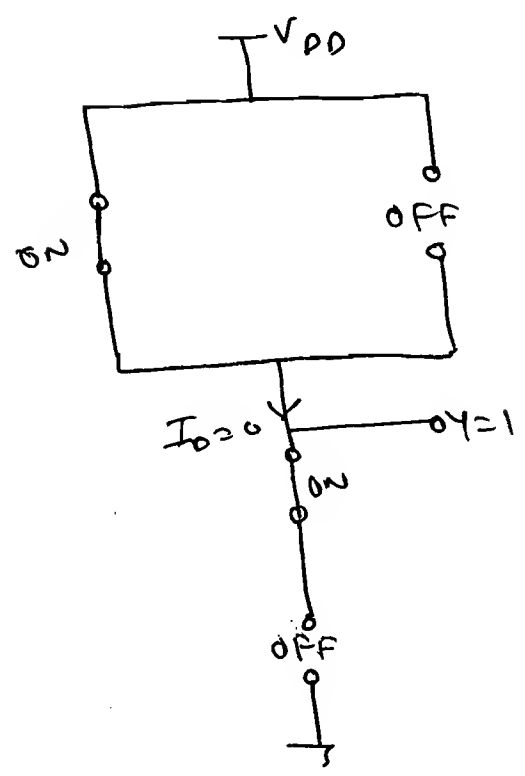
Case-(i)  $A=0, B=0$ .



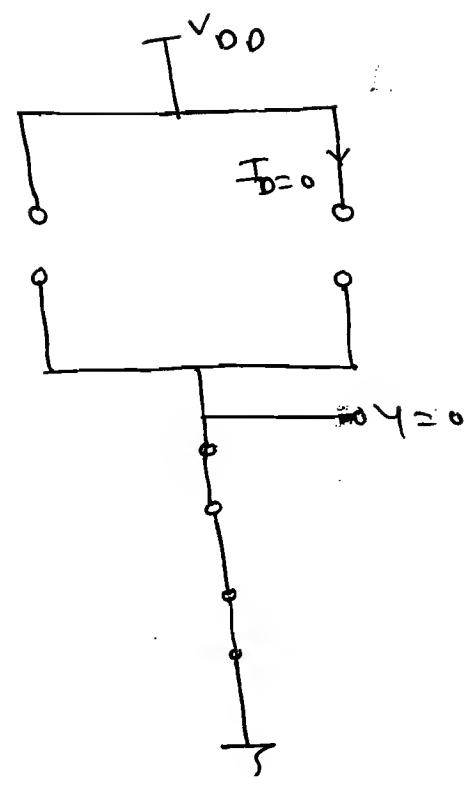
Case-(ii)  $A=0, B=1$



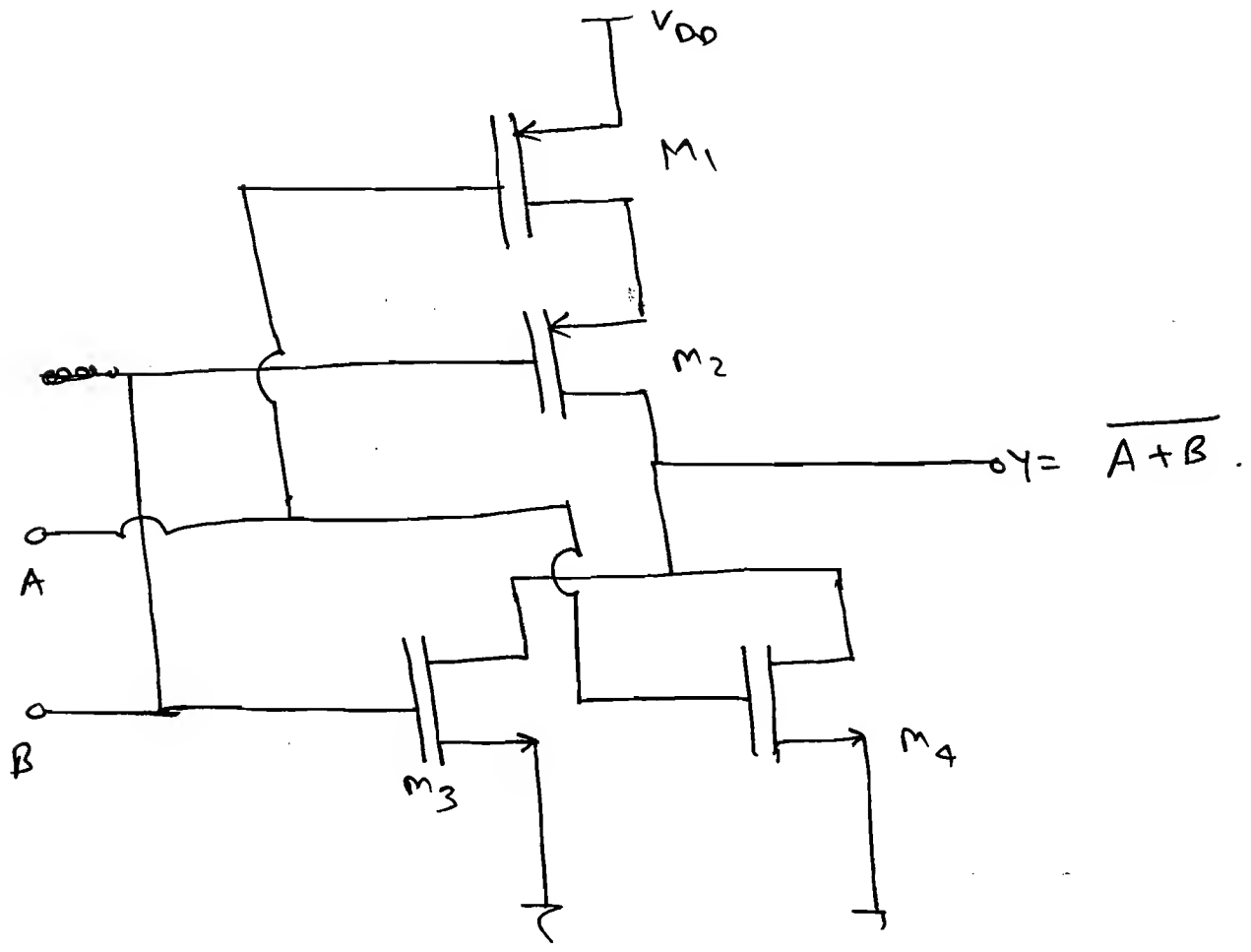
(iii)  $A=1, B=0$



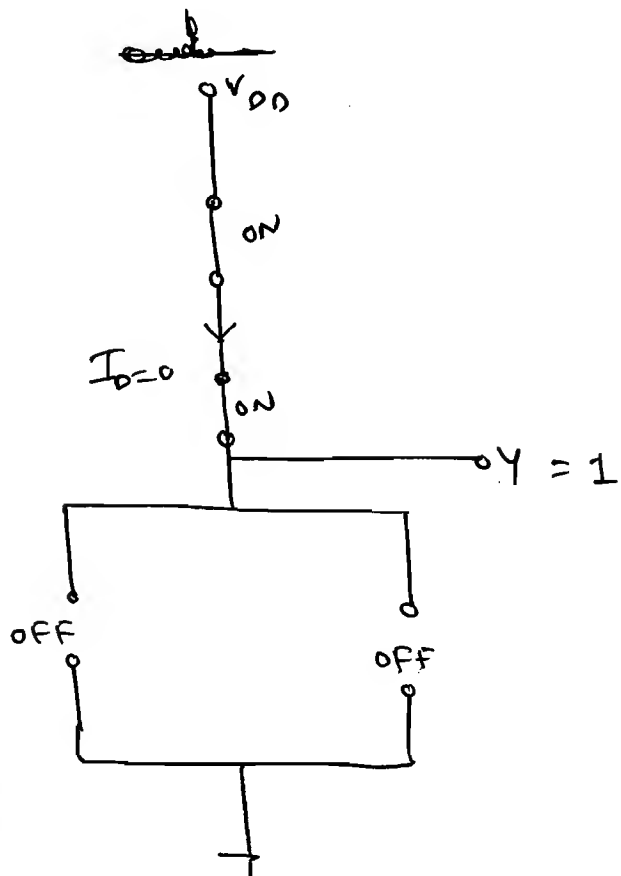
(iv)  $A=1, B=1$



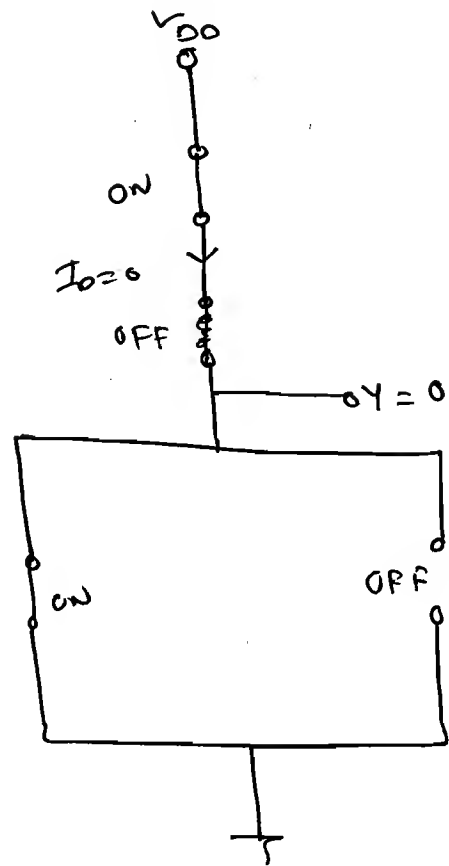
\* 2-input NOR Gate:



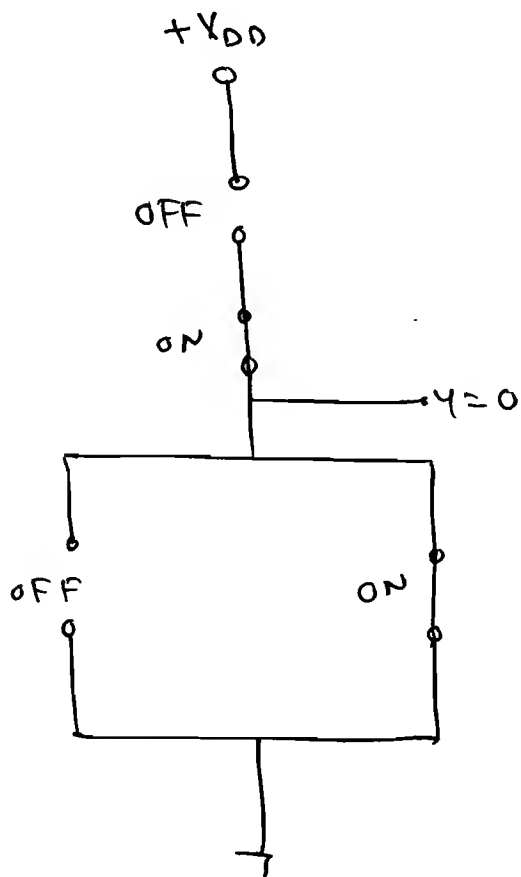
Case - (i):  $A=0, B=0$



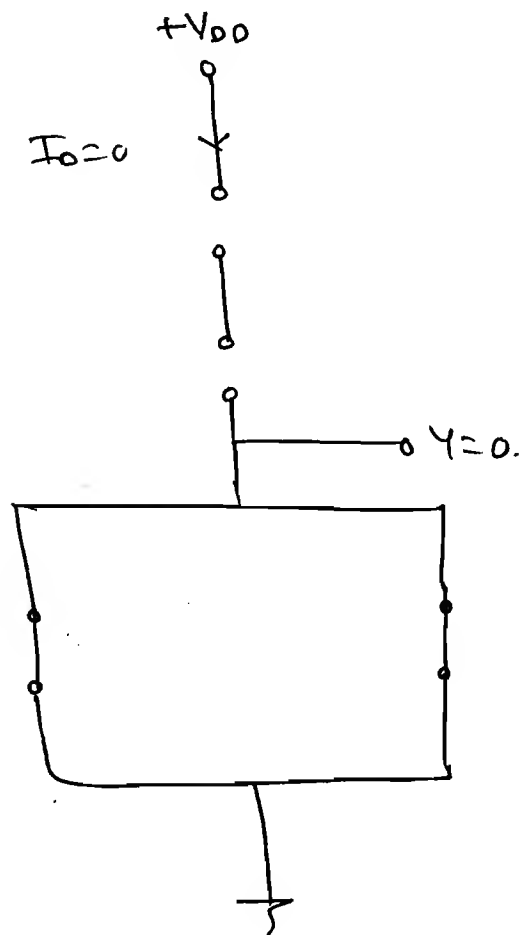
Case - ii:  $A=0, B=1$



Case - (iii):  $A=1, B=0$



Case - (iv):  $A=1, B=1$





## IMP Concept:

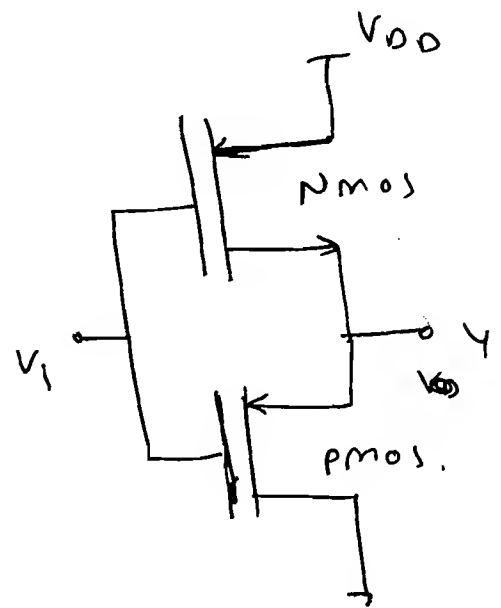
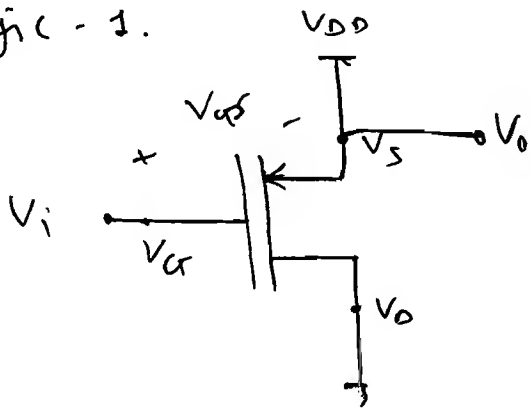
⇒ Why pmos is connected to <sup>Upside</sup> ~~VDD~~ & nmos is connected to Down in CMOS?

Ans:

⇒ Pmos Transistor passes Logic - 1 without Distortion. But it passes Logic - 0 with distortion. Therefore pmos transistors always connected to  $V_{DD}$  (or) pulled up to pass

Logic - 1.

⇒



⇒ if  $V_i = 0$ . ⇒  $V_o$  should be zero (or).

i.e. Pmos is in ON state.

for that  $V_{gs} < V_T$ .

$$\text{let, } V_T = -0.7V.$$

$$\therefore V_{gs} - V_s < V_T.$$

$$\therefore 0 - V_o < -V_T.$$

$$\therefore V_o > V_T.$$

$$\therefore |V_o| > |V_T|.$$

$$\text{i.e., } V_o > 0.7V.$$

So, instead of getting '0', we get 0.7.

So, distortion will occur.

Now, Let,  $V_i = +V_{DD} \Rightarrow$  Pmos is OFF and  $V_o$  should be  $+V_{DD}$ .

$$\therefore V_{GS} = V_G - V_S$$

$$\therefore V_{GS} = V_{DD} - V_{DD} = 0$$

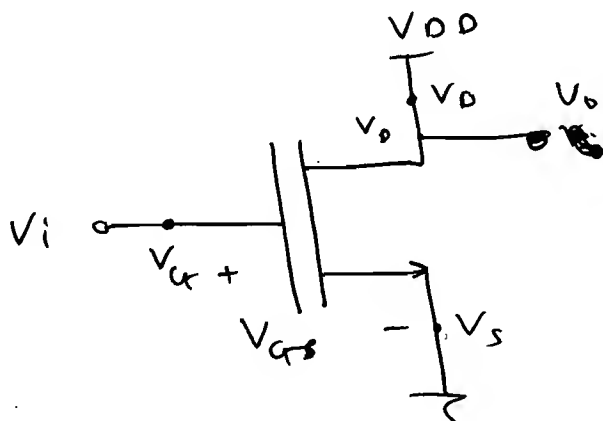
$V_{GS} = 0 \Rightarrow V_G \neq V_{DD}$ . Pmos is OFF and

$V_S = V_o = +V_{DD}$  perfect.

So, Pmos passes Logic '1' without distortion and passes Logic '0' with distortion.

$\Rightarrow$  Nmos:

$\rightarrow$  Nmos Transistor passes Logic-0 without distortion and passes Logic-1 with distortion. Therefore Nmos Transistor always connected to ground (or) pulled down to pass Logic-0.



$\Rightarrow$  In order to get  $V_o = +V_{DD}$ ,  $V_i = 0 \Rightarrow$  in cut-off.

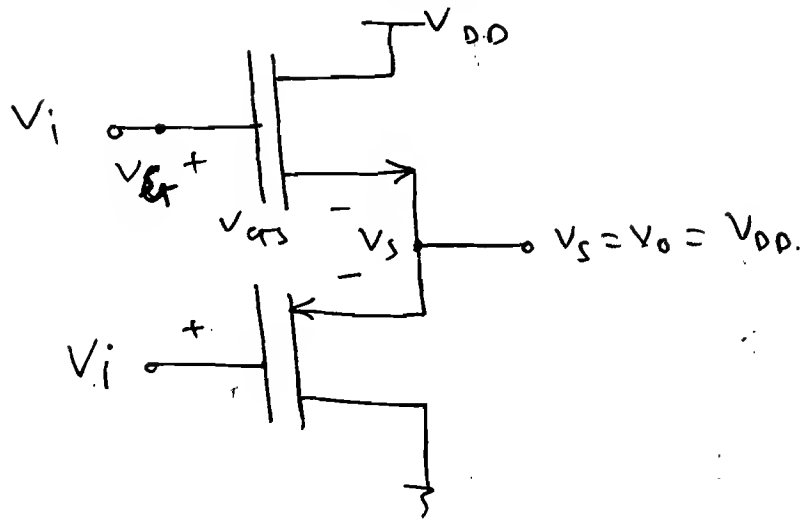
But for cut-off  $V_{GS} < V_T$ . let  $V_T = 0.7V$

$$\therefore V_G - V_S < 0.7$$

$$\therefore V_G < 0.7$$

so,  $V_i$  should be  $> 0.7$ .

$\Rightarrow$  Now, if NMOS is connected to HP-side then,



$\Rightarrow$  Now, if  $V_i = 0$  then  $V_S = V_0 = +V_{DD} = +5V$  for inverter.

In order to get  $V_S = V_0 = +V_{DD} = +5V$  NMOS should be in cut off. Sat.

$\therefore V_{GS} \leq V_T$ , Let  $V_T = 0.7V$ .

$\therefore V_G - V_S \leq 0.7$ .

$\therefore 0 - V_S \leq 0.7$ .

$\therefore V_S \geq -0.7$ .

~~$-5 < -0.7$~~   $\boxed{-5 > 0.7} \rightarrow$  not possible

So, we get  ~~$V_0 = 1.3$  instead of  $V_{DD}$~~ .

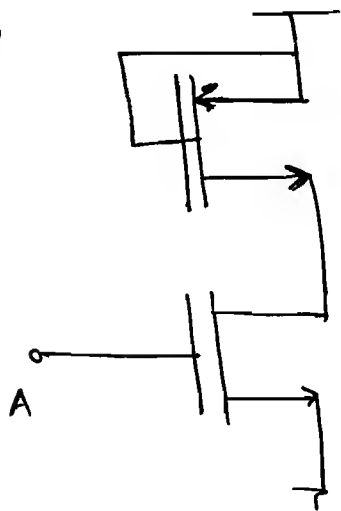
So we get distortion. n-mos is OFF.

$\Rightarrow$  So, NMOS Transistor passes Logic-0 without distortion. But it passes Logic-1 with distortion. Therefore NMOS Transistor always connected to ground (or) pulled down to pass Logic-0.

# ★ Inverters:

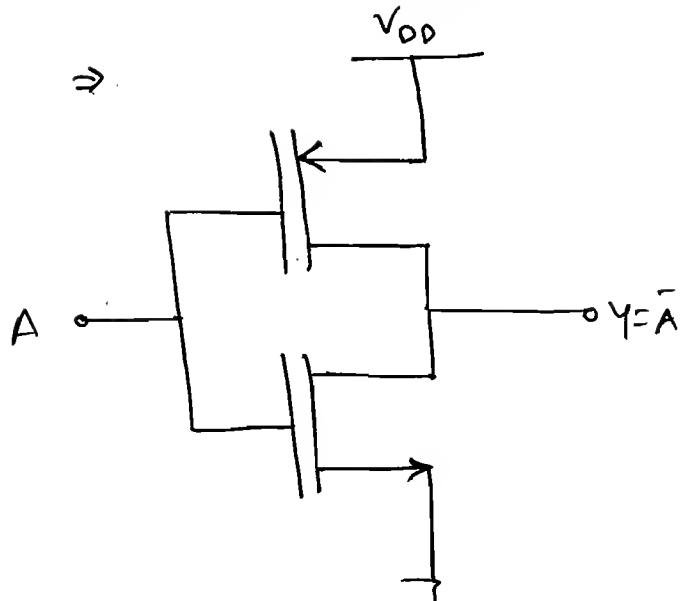
n-MOS

⇒



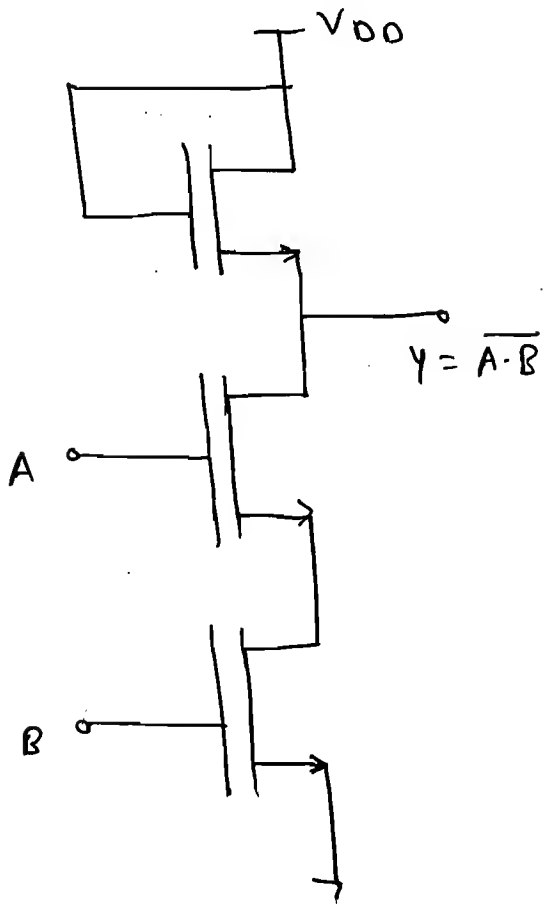
CMOS:

⇒

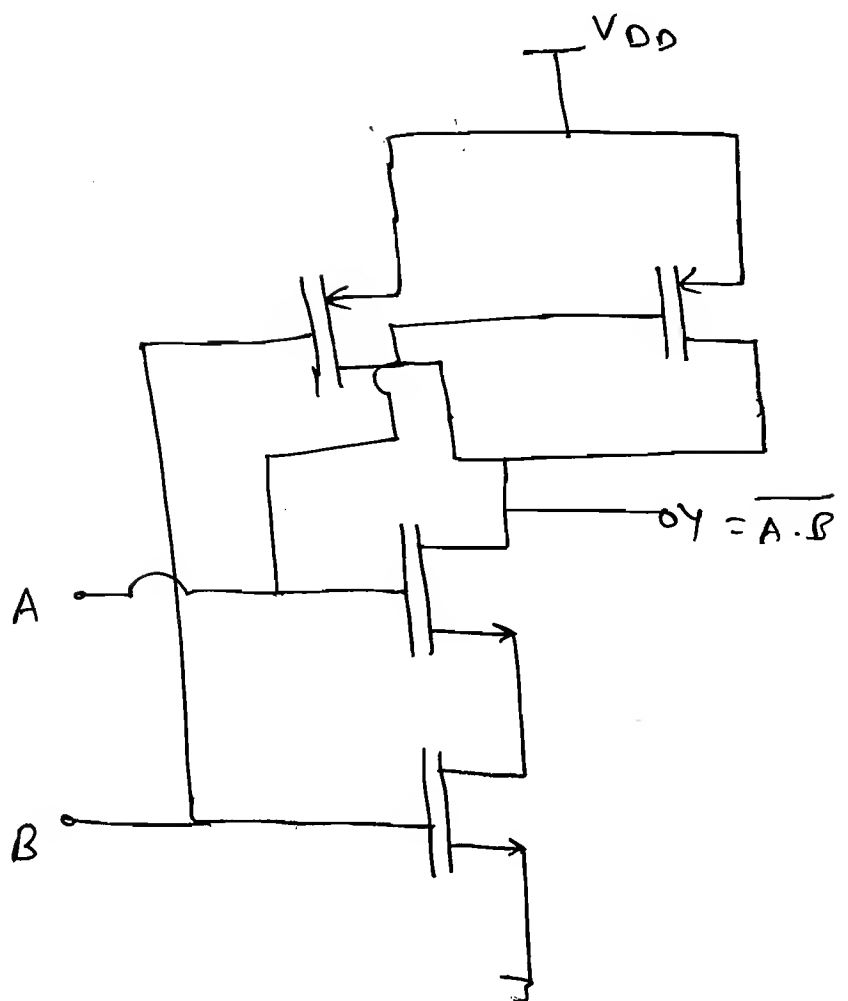


# ★ 2 i/p NAND gate:

n-MOS

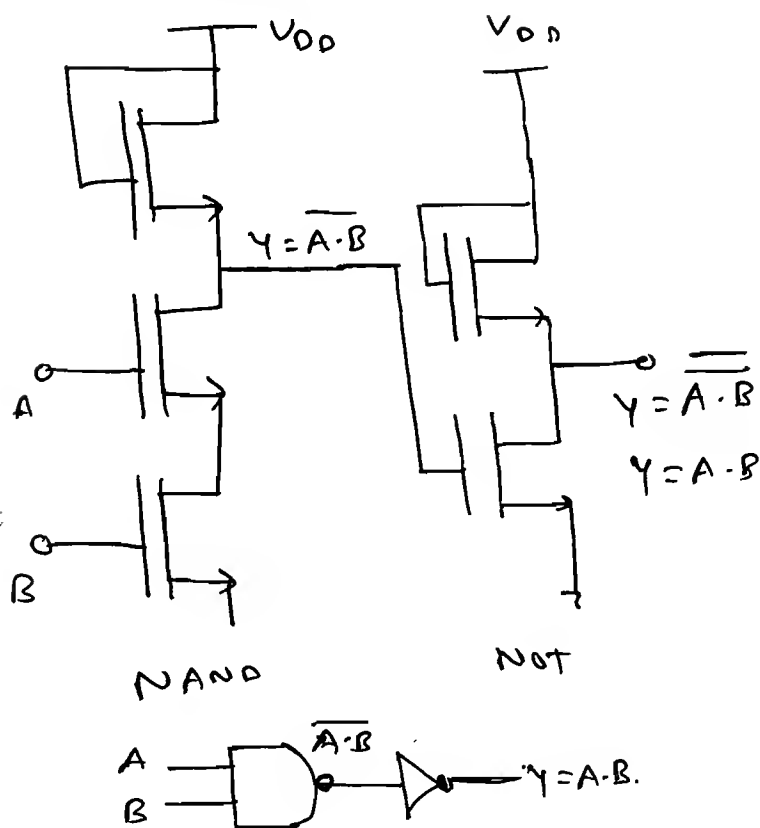


CMOS:

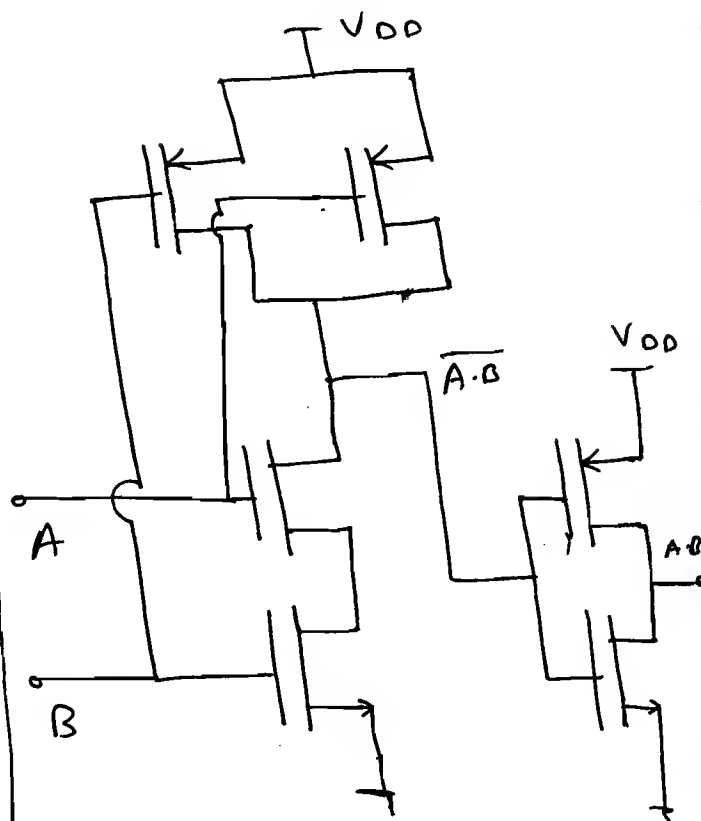


# \* 2-Input AND Gate:

Nmos:



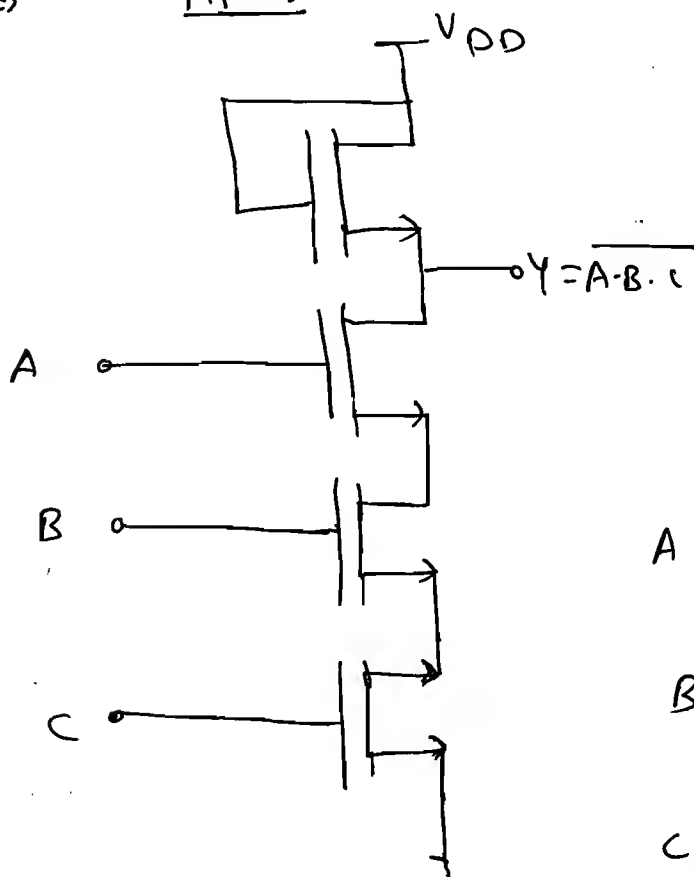
CMOS:



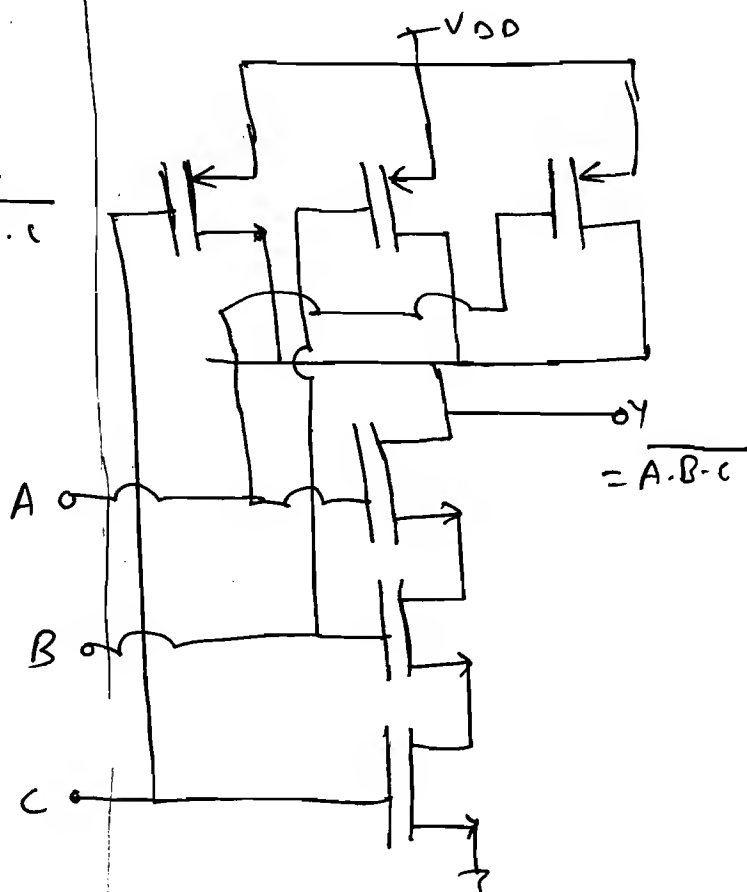
# \* 3-Input NAND Gate:

⇒

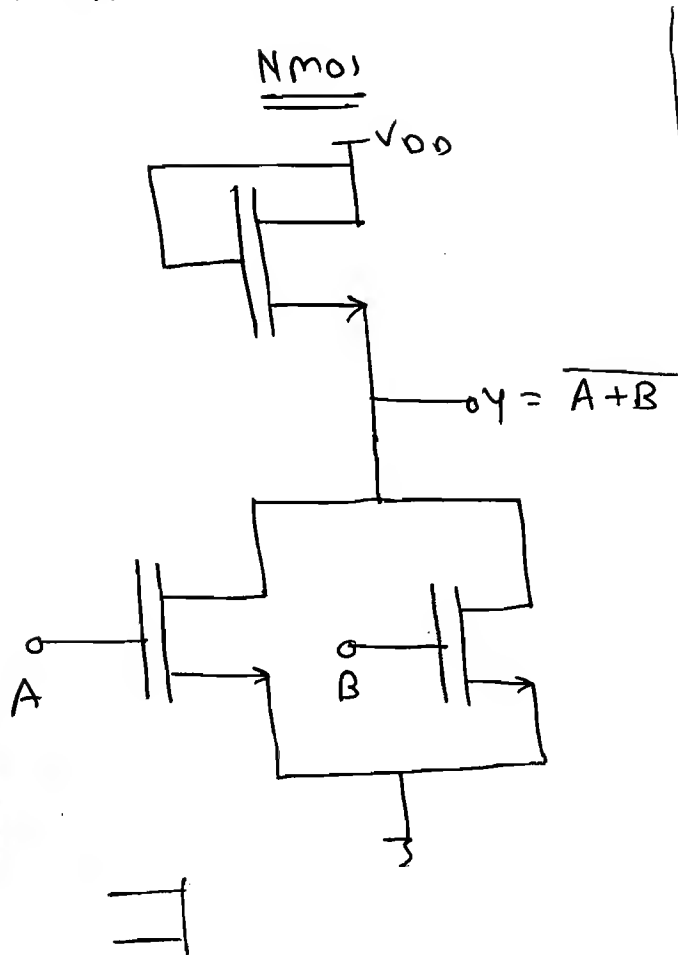
Nmos:



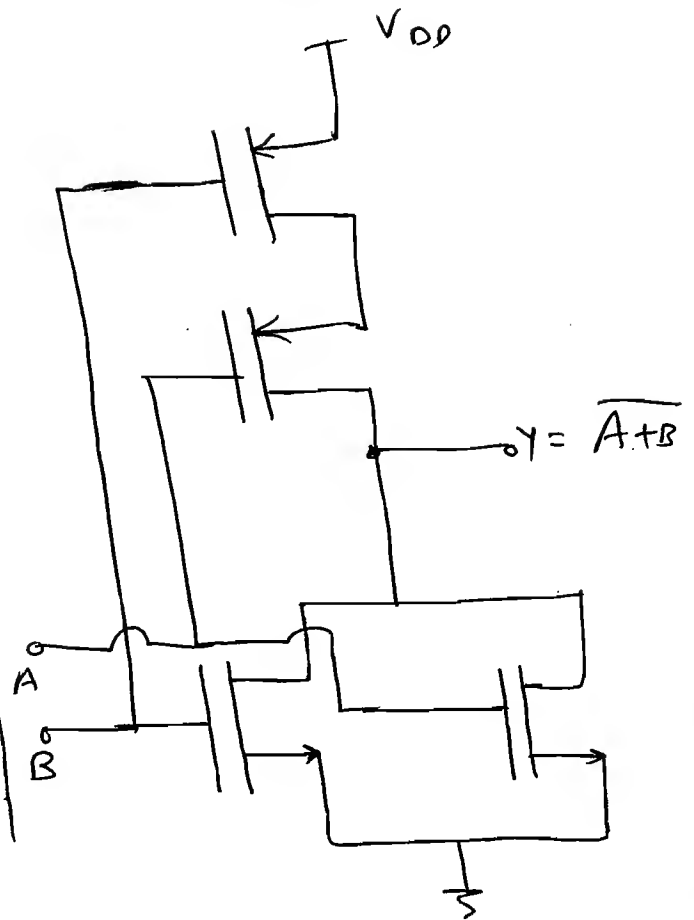
CMOS:



\* 2 I/P NOR gate:

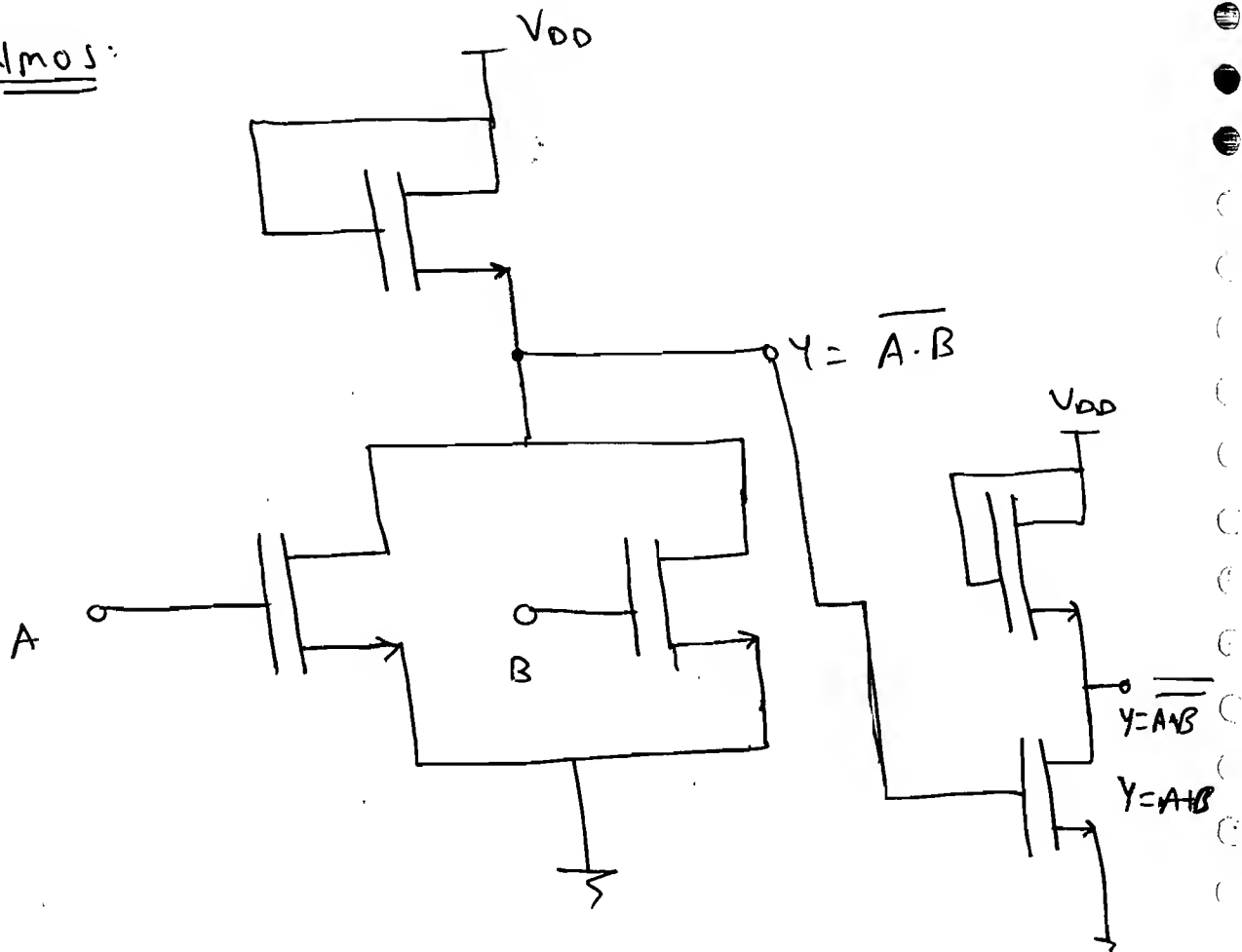


CMOS

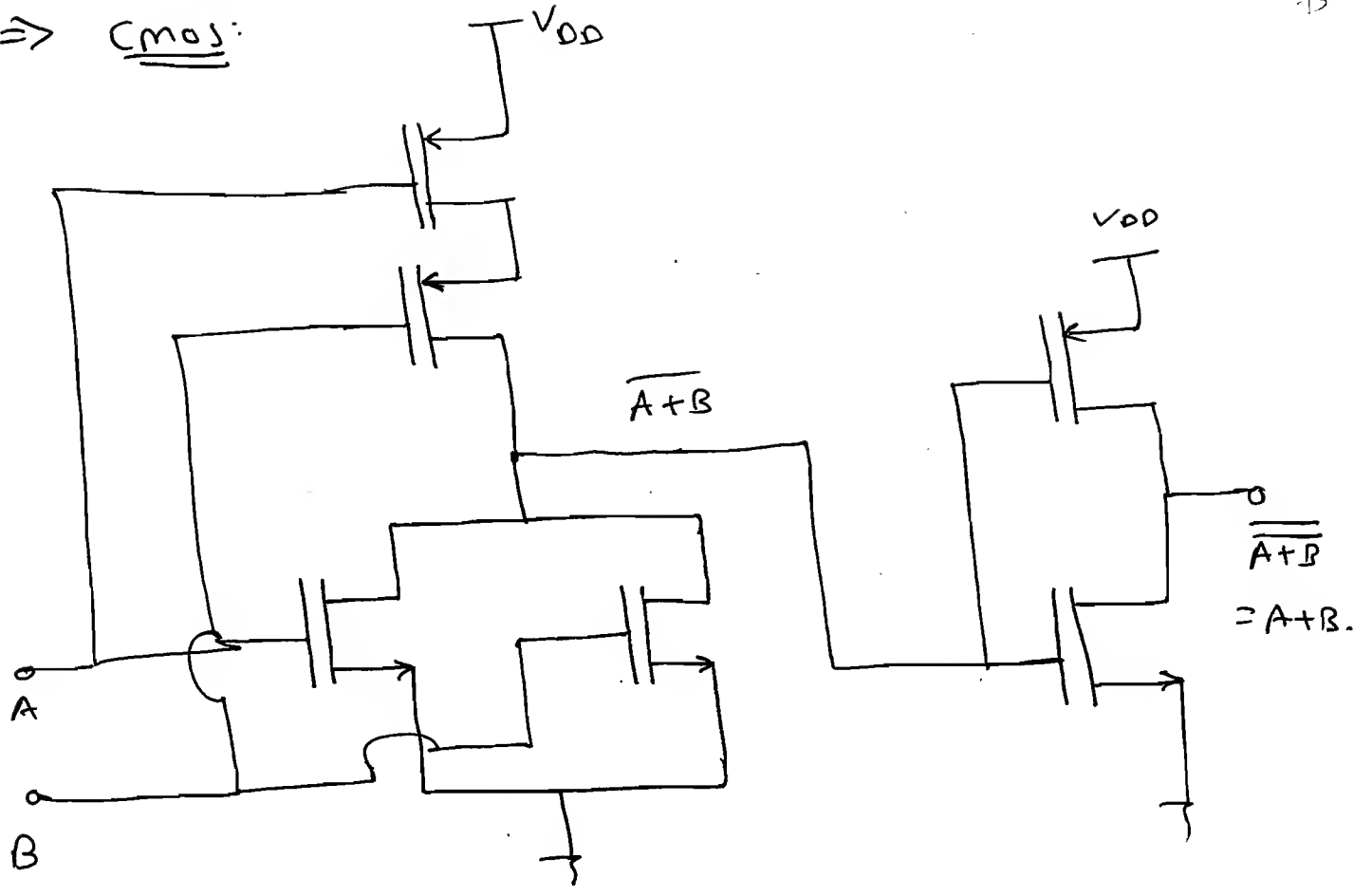


\* 2 I/P OR gate:

Nmos:

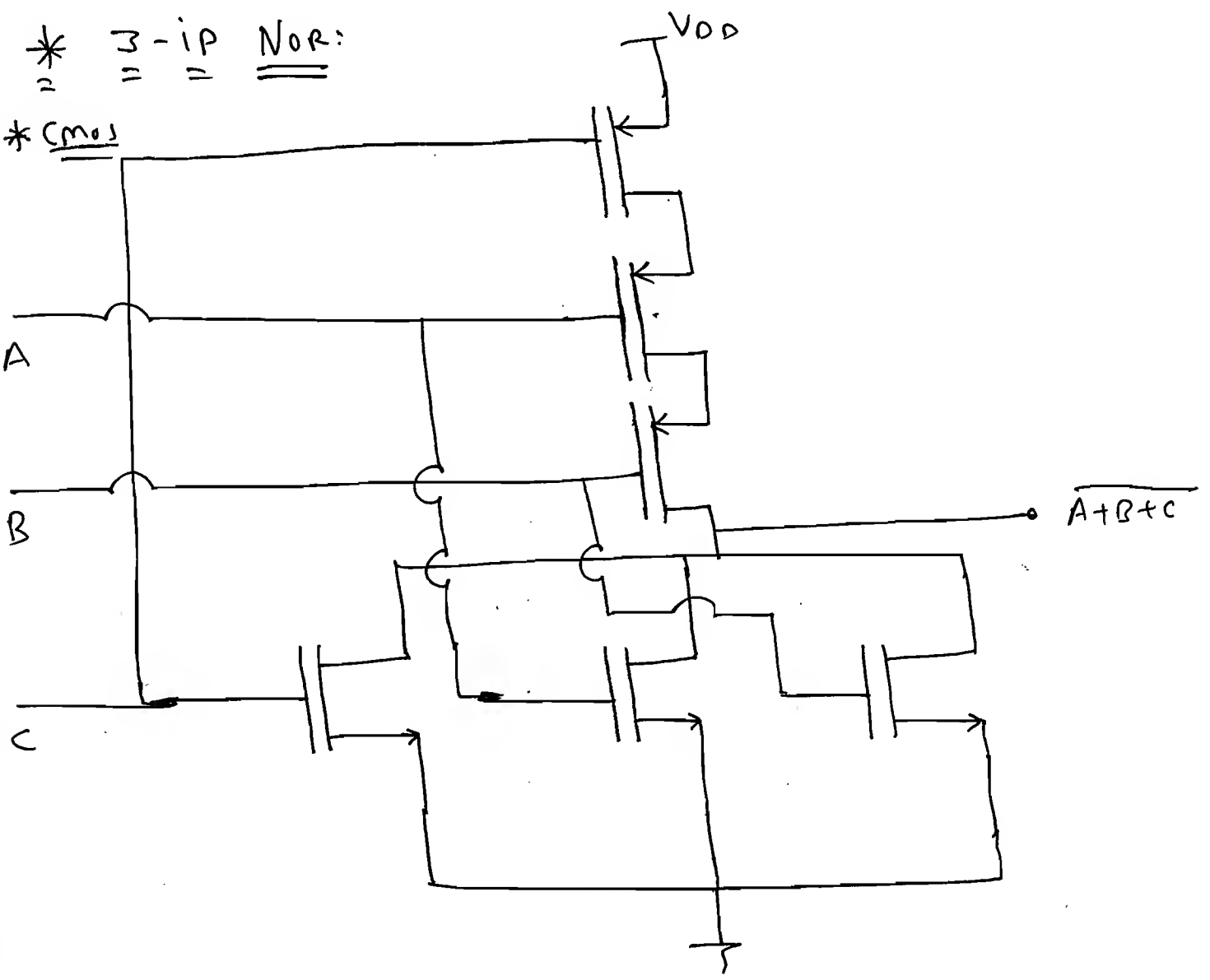


$\Rightarrow$  Cmos:

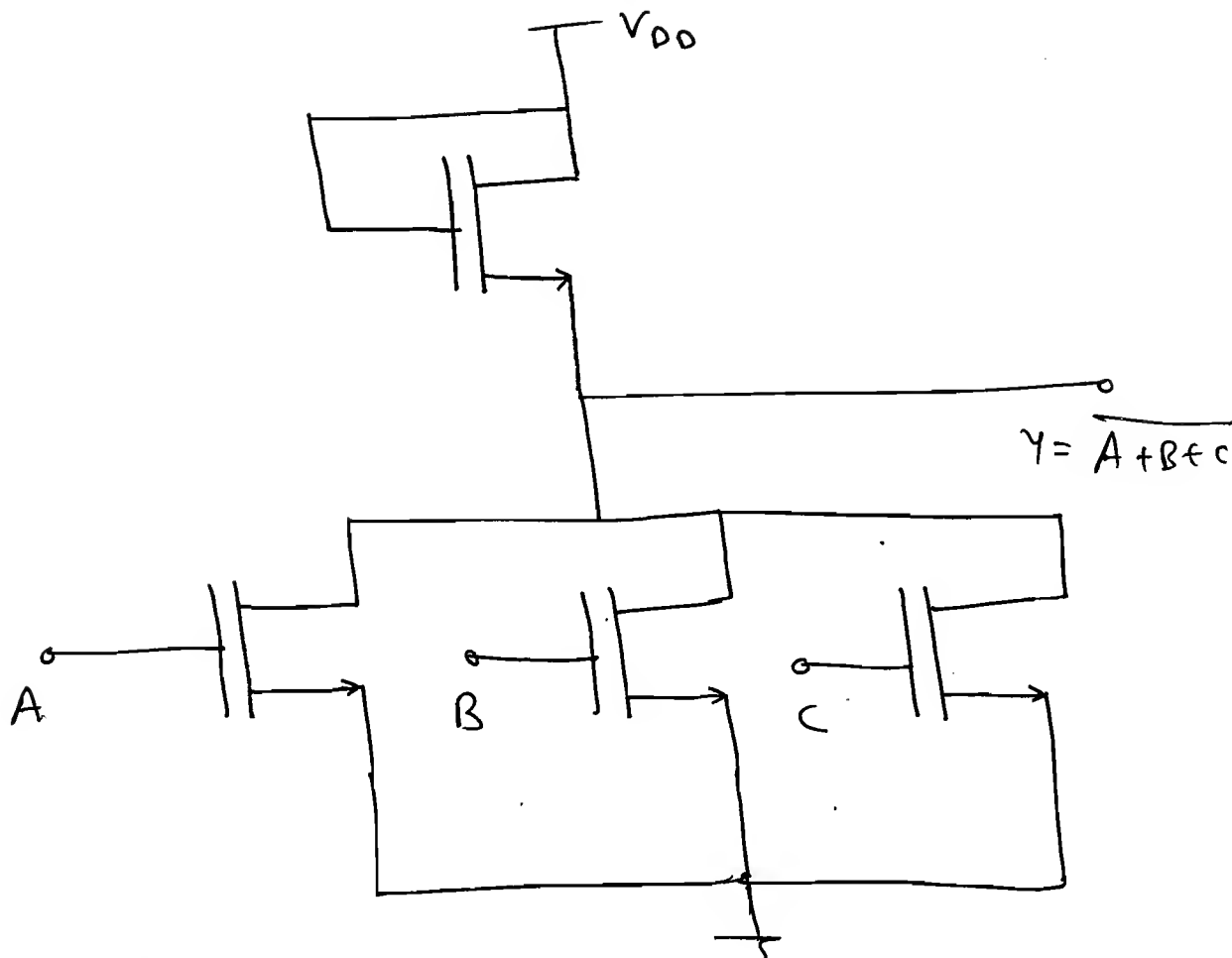


\* 3-ip NOR:

\* Cmos



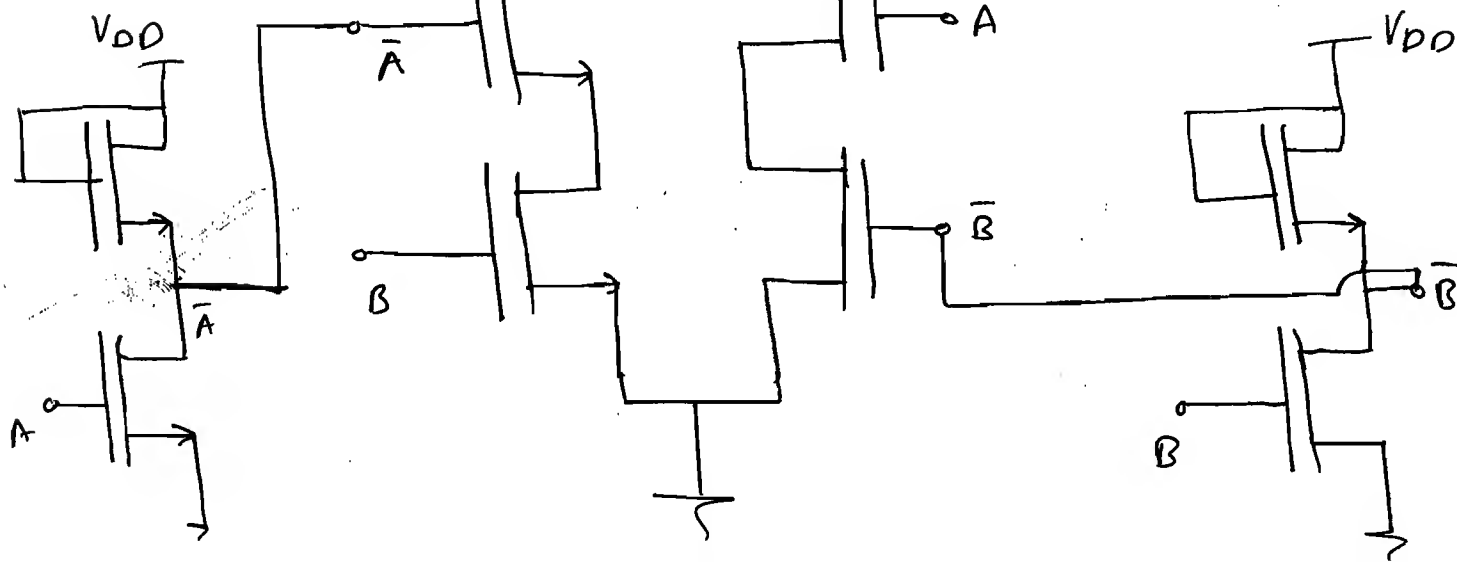
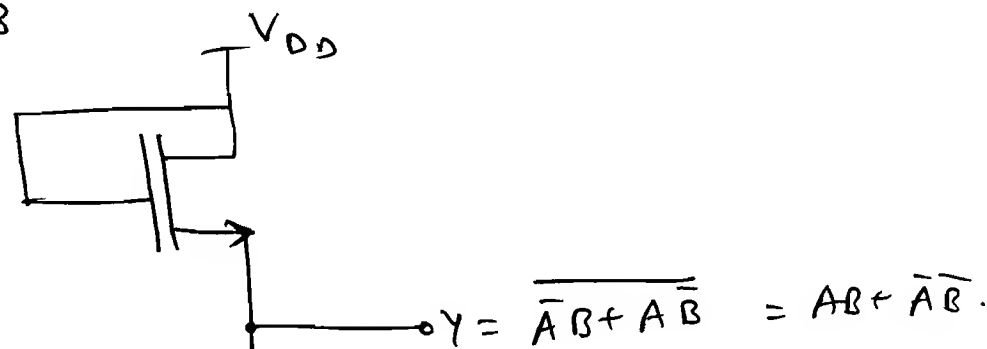
\* Nmos:



\* 2-input ~~XNOR~~ gate:

$$Y = A \odot B = \overline{AB + A\bar{B}}$$

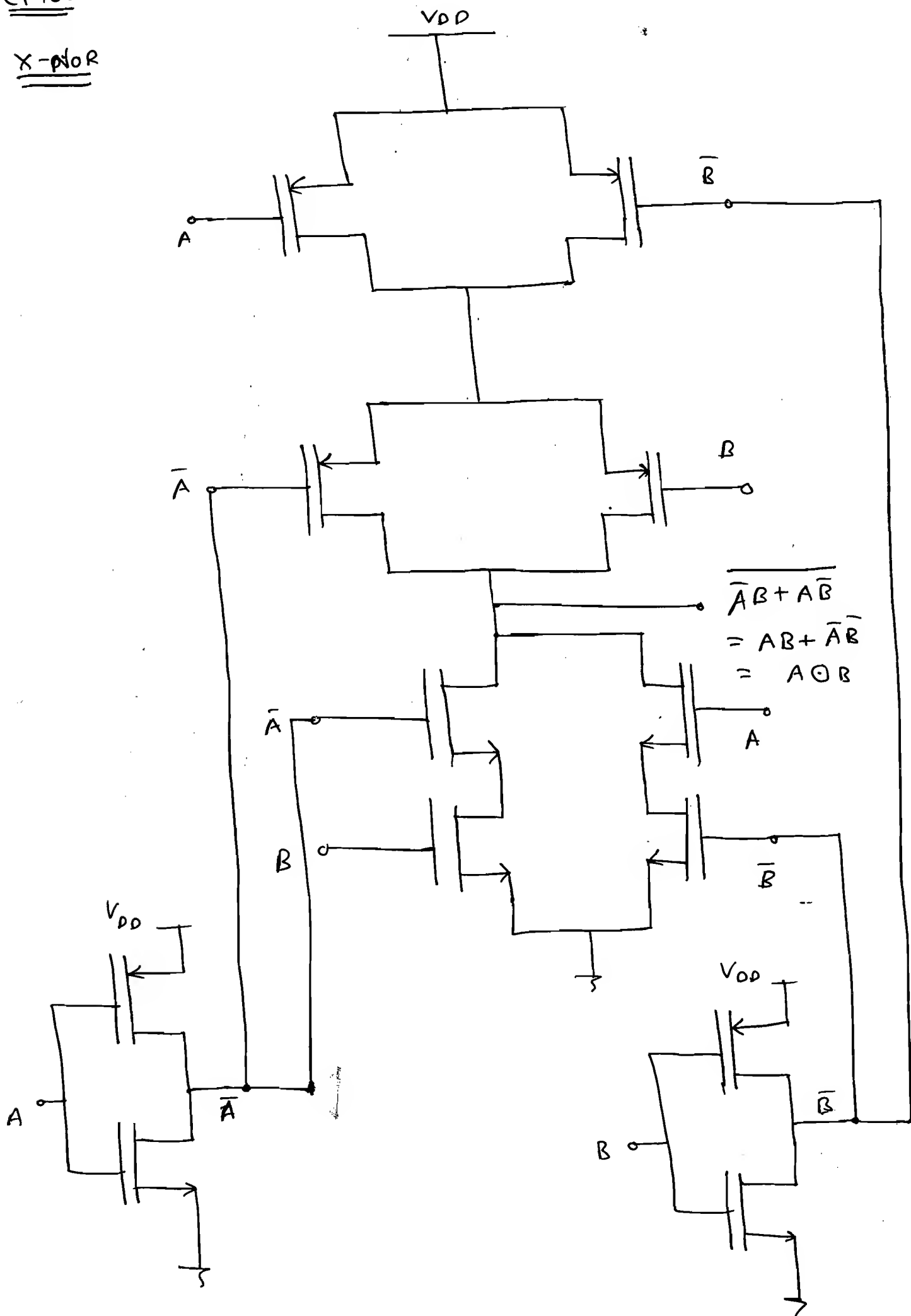
$$Y = AB + \bar{A}\bar{B}$$





CMoS:

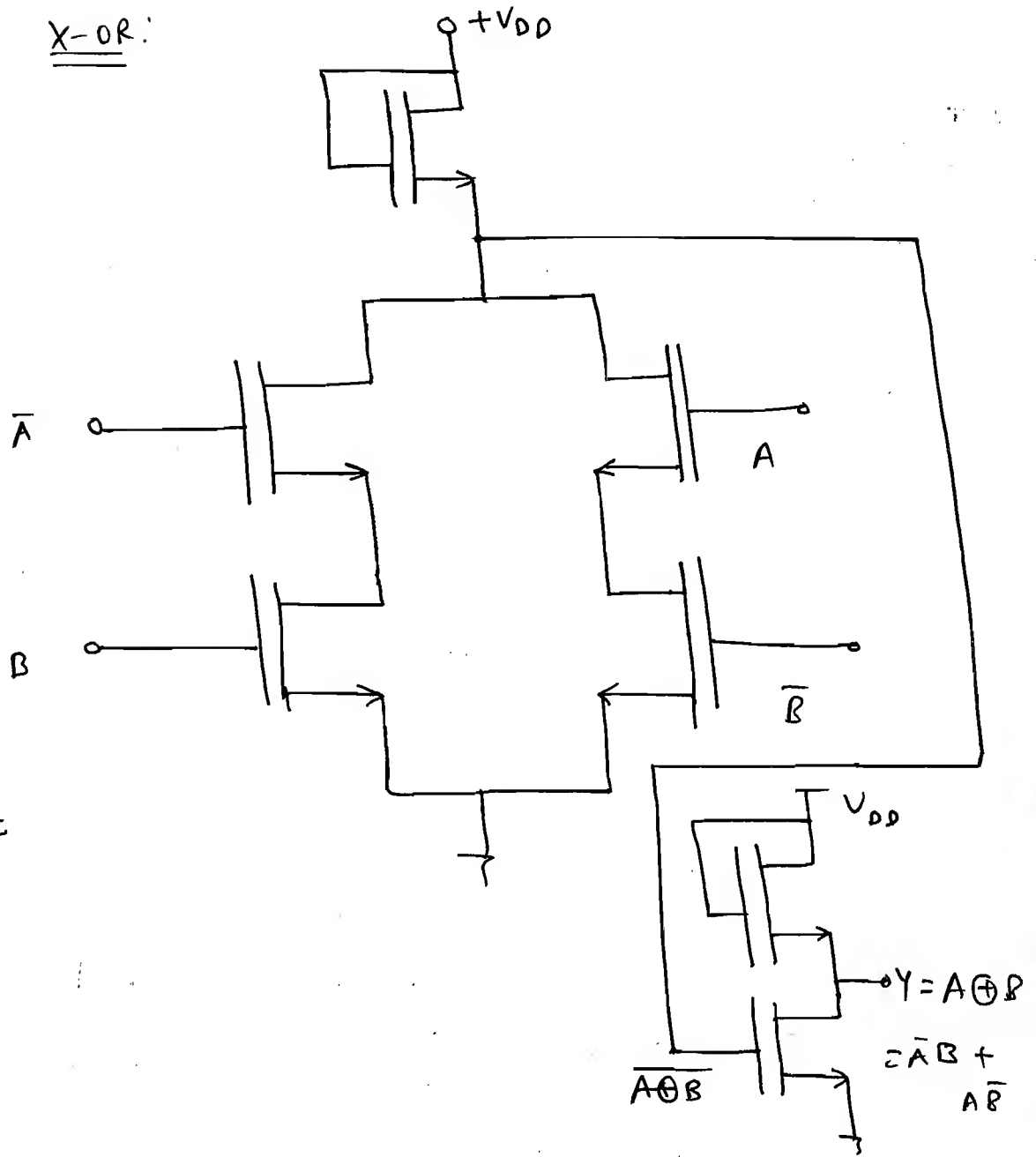
X-NOR



\* 2 I/P    X-OR:

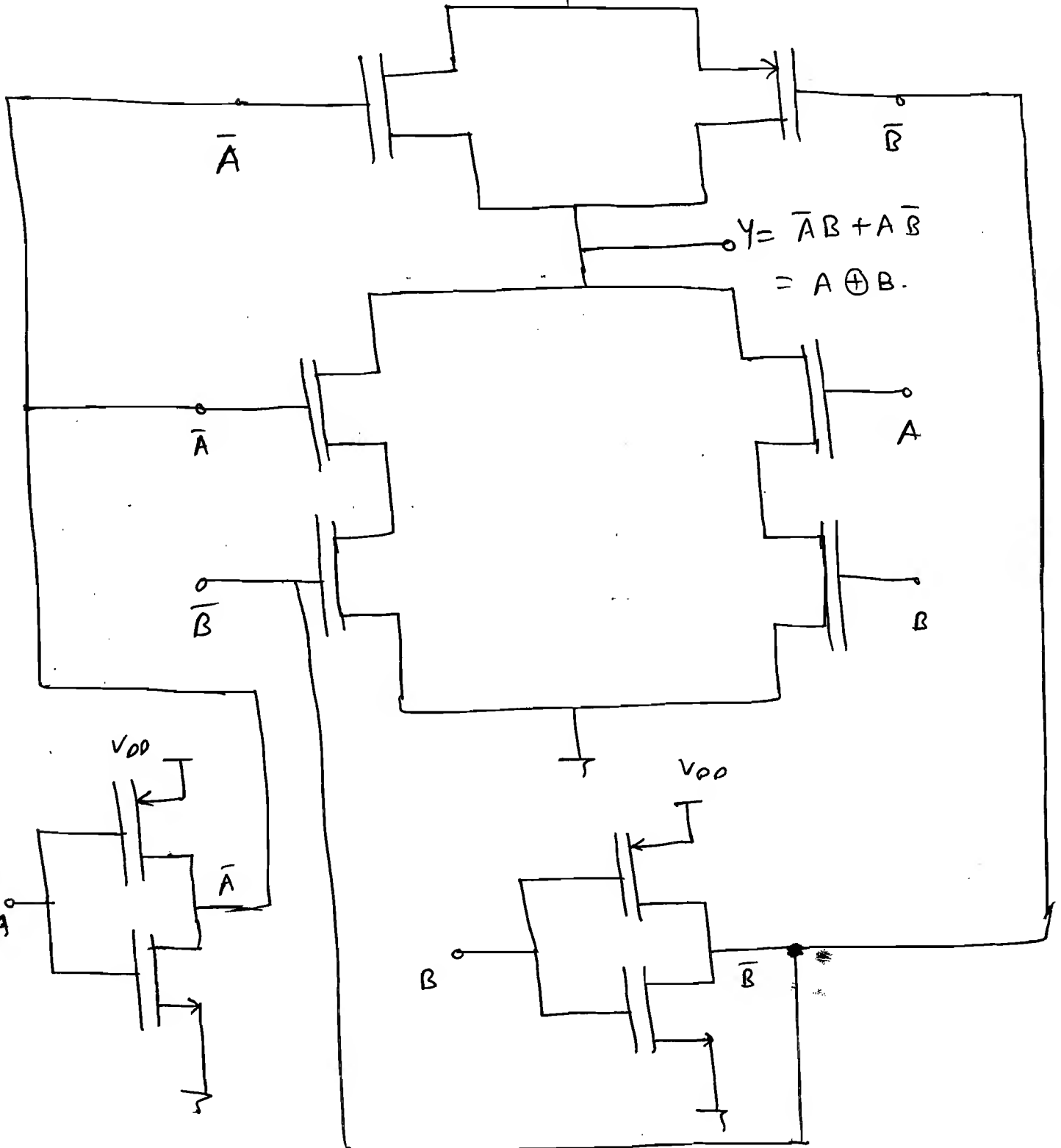
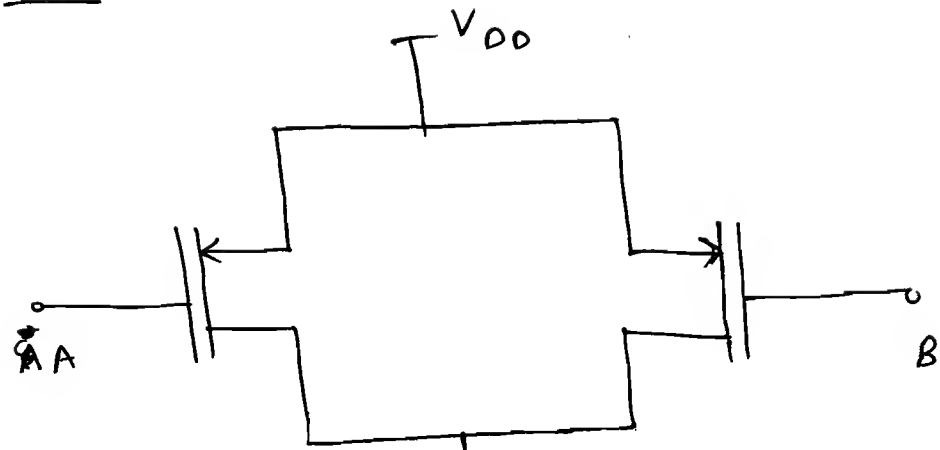
$$Y = \bar{A}B + A\bar{B}$$

Nmos



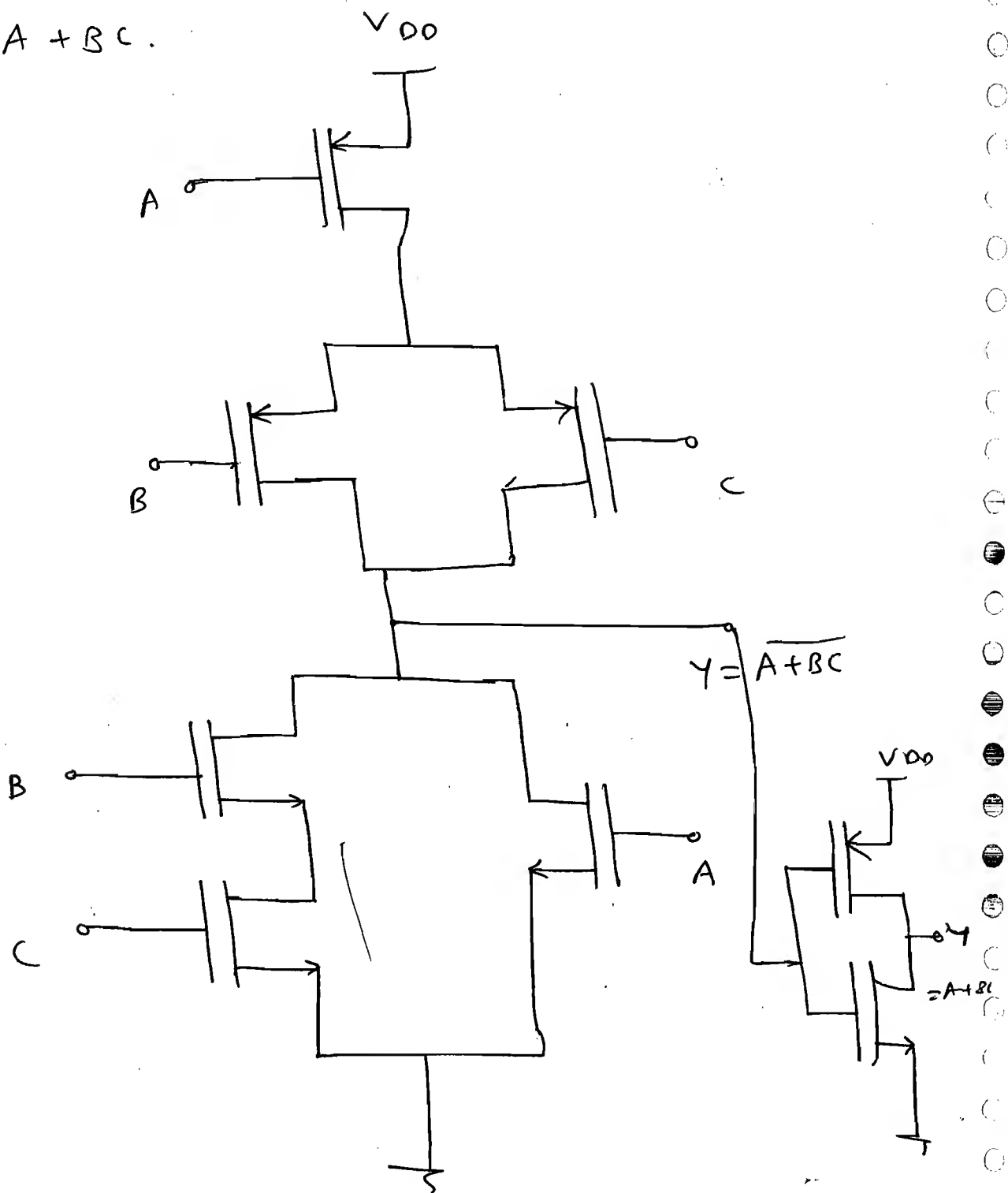
\* 2-11p X-OR :

Cmos:



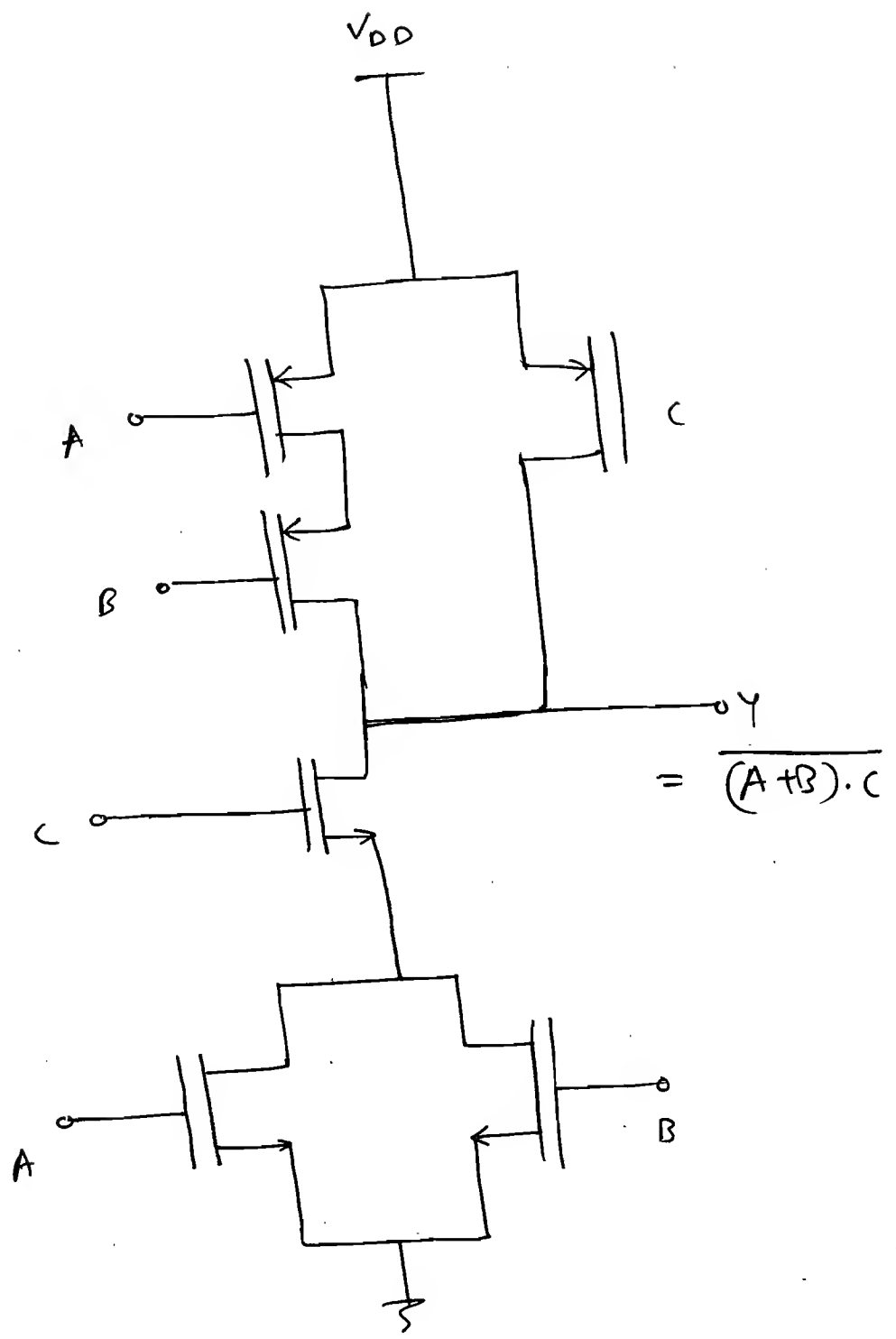
\* Implement the following fn in CMOS technology:

①  $Y = A + BC$ .

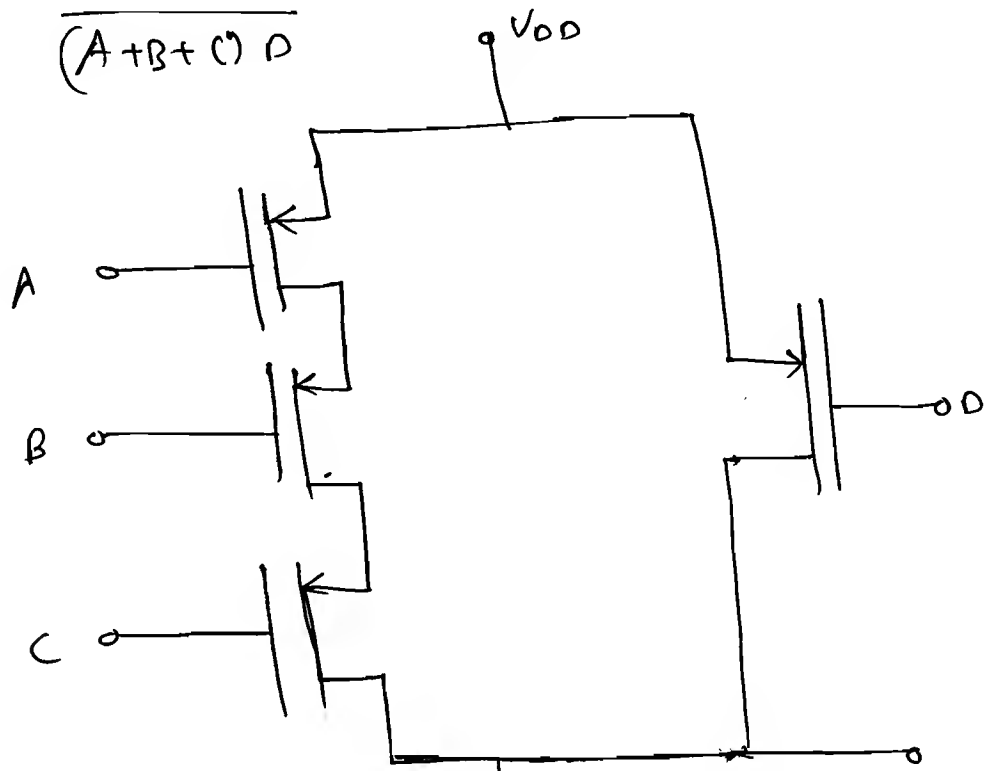


②  $Y = \overline{(A+B) \cdot C}$

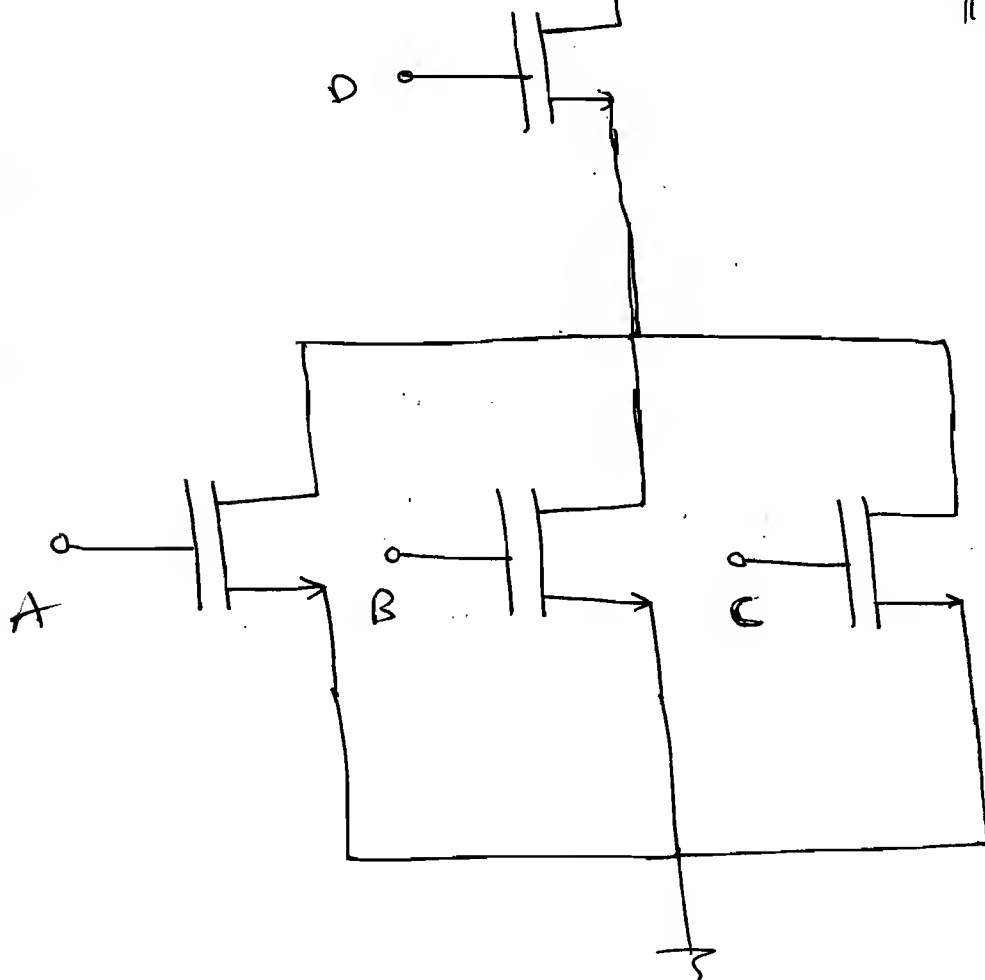
$\Rightarrow$



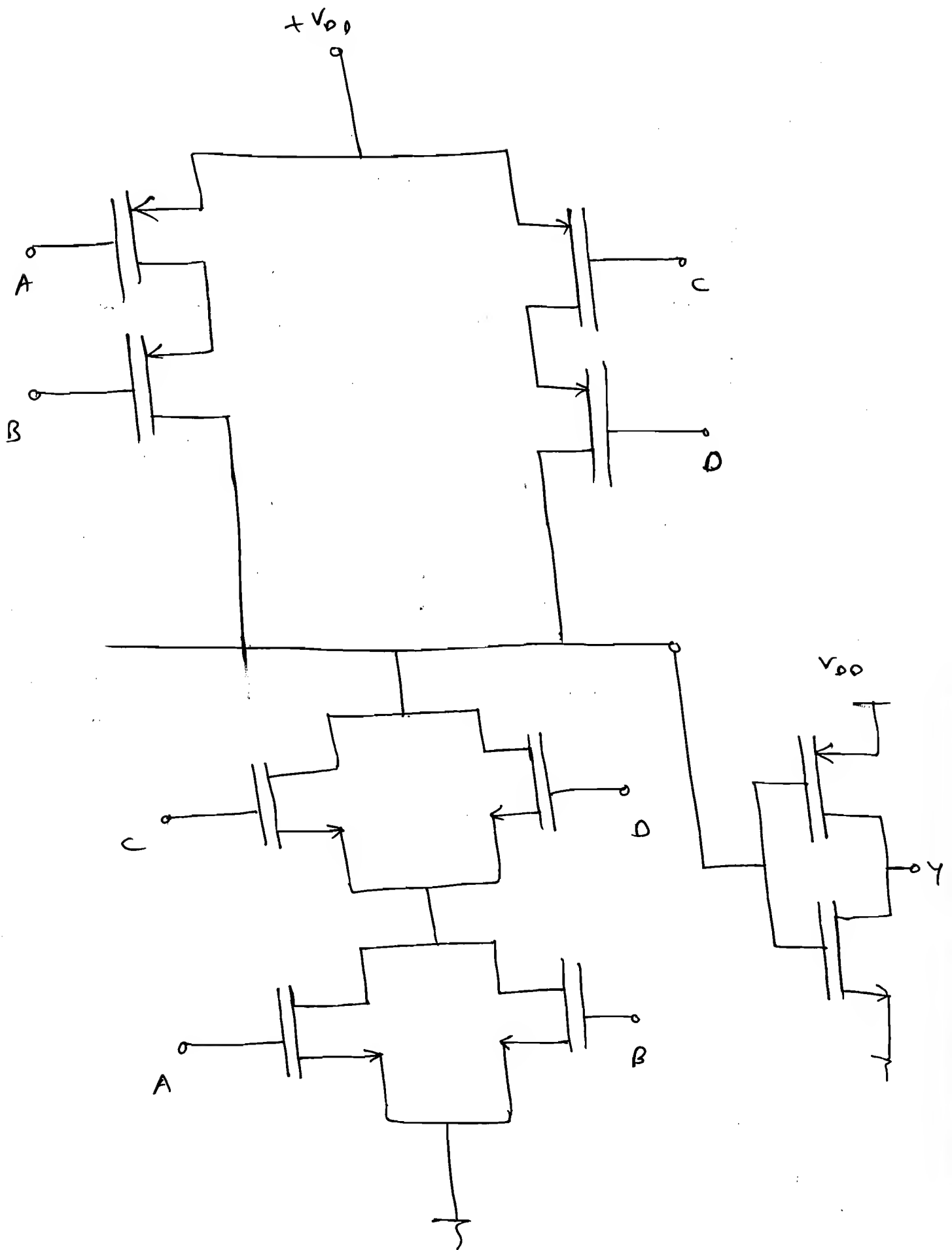
3.  $Y = \overline{(A+B+C)D}$



$Y = \overline{(A+B+C)D}$

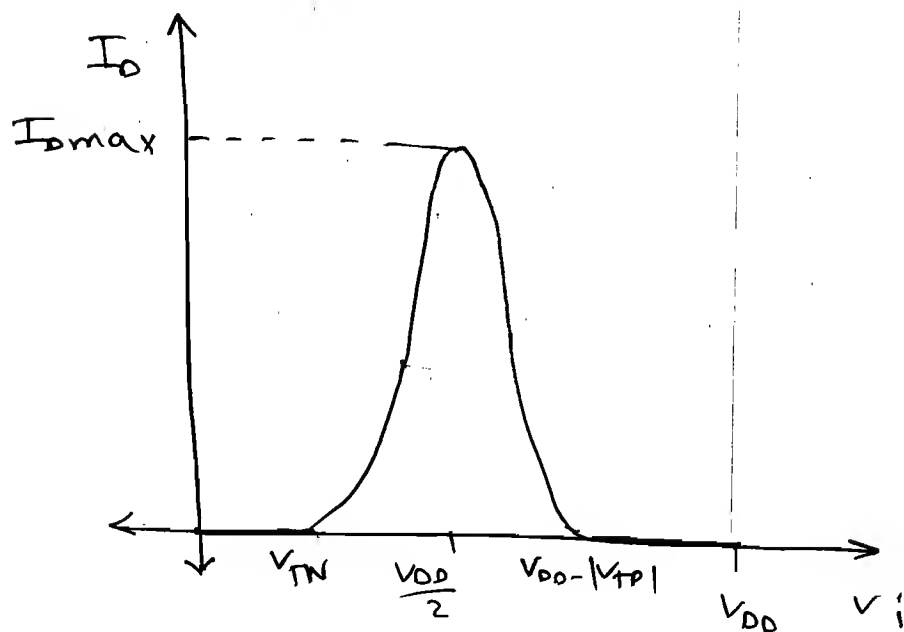
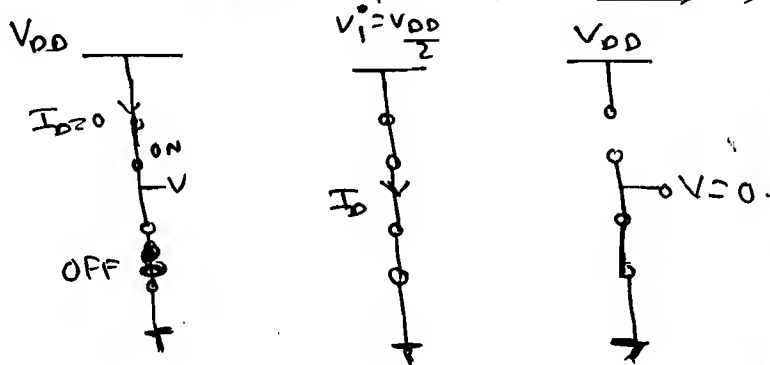
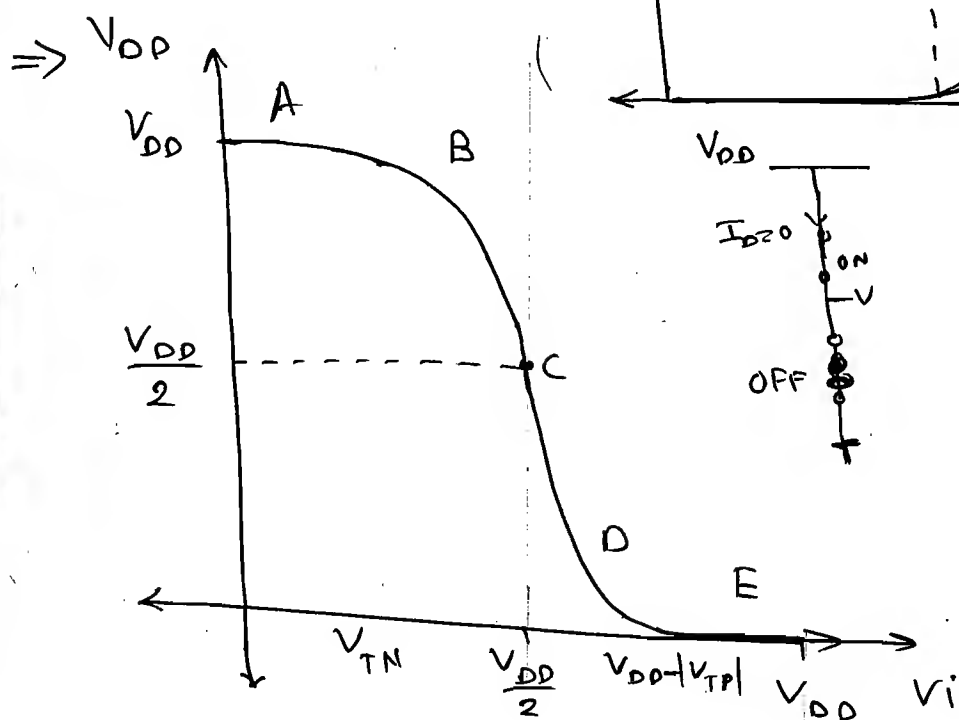
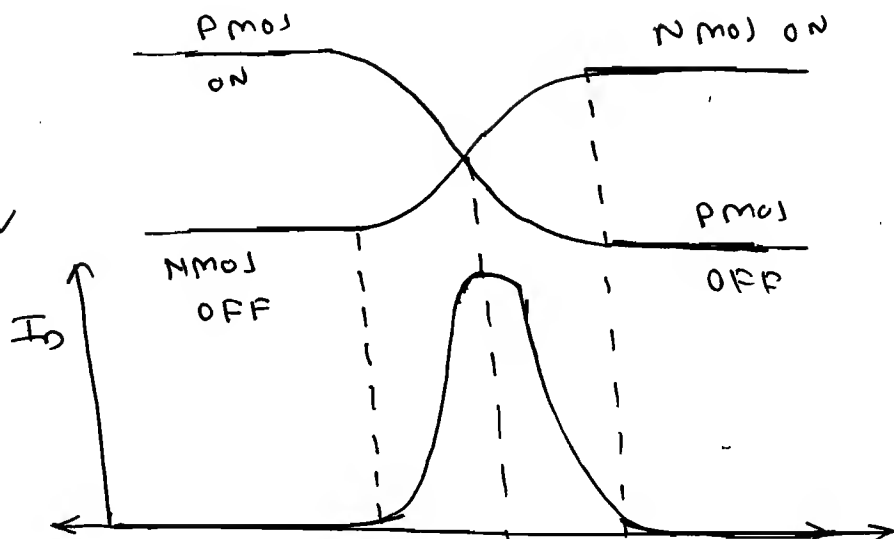
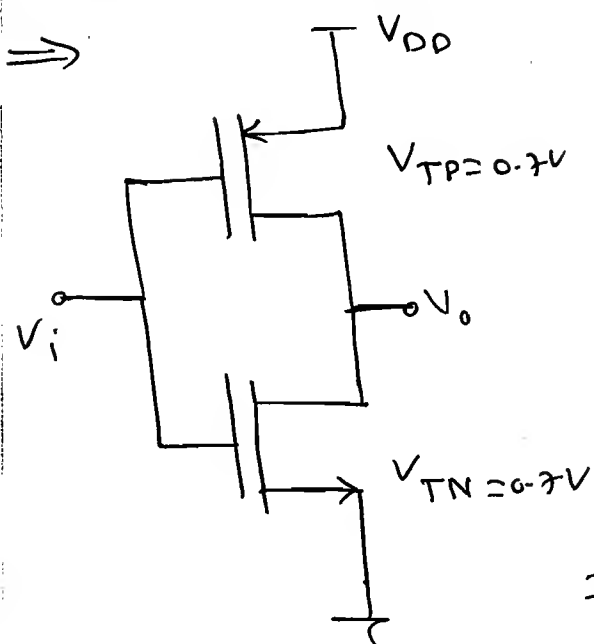


4.  $Y = (A+B)(C+D)$ .



# ☆ Transfer characteristics of An Inverter:

IMP





Reg	Condition	PMOS	NMOS	output
A	$0 < V_i < V_{TN}$	Linear	cut-off	$V_o = V_{DD}$
B	$V_{TN} < V_i < V_{DD}/2$	Linear	Sat	$V_o > \frac{V_{DD}}{2}$
C	$V_i = V_{DD}/2$	Sat	Sat	$V_o = \frac{V_{DD}}{2}$ <small>deep shorting</small>
D	$\frac{V_{DD}}{2} < V_i < V_{DD} -  V_{TP} $	Sat	Linear	$V_o < V_{DD}/2$
E	$V_i > V_{DD} -  V_{TP} $	cut-off	Linear	$V_o = 0$

①  $0 < V_i < V_{TN} \therefore$

$\Rightarrow V_i = 0.5V$

$V_{GS} = V_G - V_S$

$V_{GS} = 0.5$

$V_{GS} = 0.5 < (V_{TN} = 0.7V)$

So, OFF

PMOS

$V_i = 0.5V$

$V_{GS} = V_G - V_S$

$= 0.5 - 5 = -4.5$

$\therefore V_{GS} = -4.5 < V_{TP}$

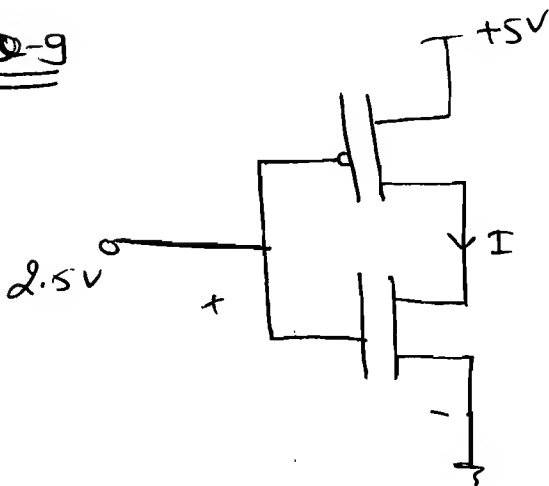
Now,  $V_{DS} = V_D - V_S$   
 $= V_{DD} - V_{DD} = 0$

$V_{DS} = 0$

$V_{GS} - V_T = -4.5 - (-0.7) = -3.8 < V_{DS}$

$V_{DS} > V_{GS} - V_T \Rightarrow \text{linear}$

Q-9



$K_n = K_p = \mu_n C_{ox} \cdot \frac{W_n}{L_n}$

$= \mu_p \cdot C_{ox} \cdot \frac{W_p}{L_p} = 40 \mu A/V^2$

$V_{GS} = 2.5V$

$V_T = 1V$

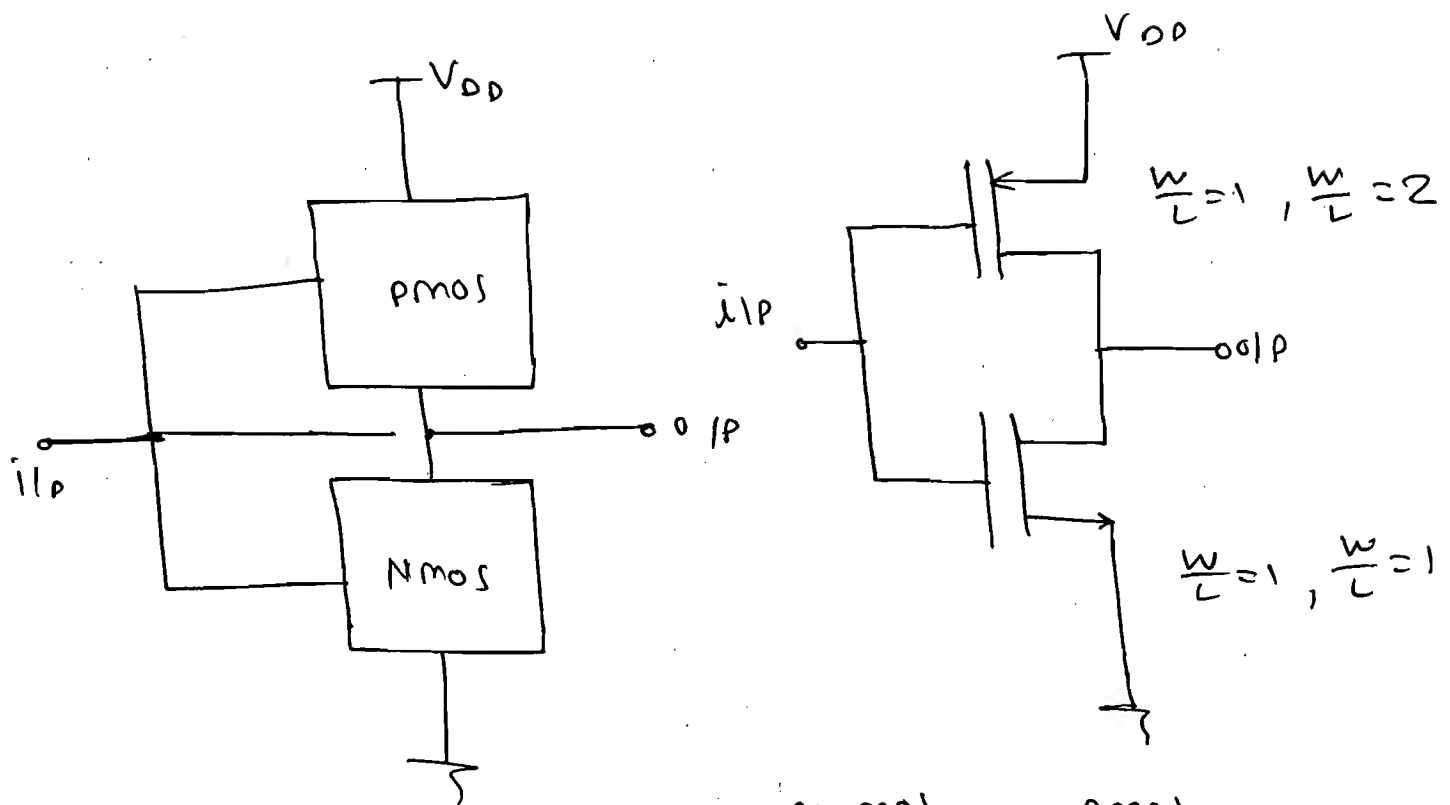
Soln.

$I_D = \frac{1}{2} \mu_n C_{ox} \cdot \frac{W_n}{L_n} [V_{GS} - V_T]^2$

$= \frac{1}{2} \times 40 \times 10^{-6} [2.5 - 1]^2 = 20 \times 10^{-6} \times 2.25$

$I = 45 \mu A$

# \* Transistor Sizing:



n-mos

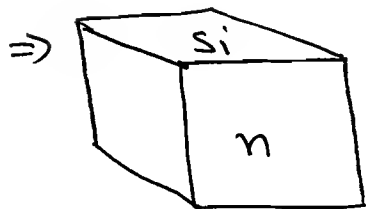
$$L = 1 \mu m$$

$$W = 1 \mu m$$

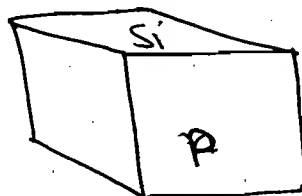
p-mos

$$L = 1 \mu m$$

$$W = 1 \mu m$$



$$\sigma_n = n \mu_n q$$



$$\sigma_p = p \mu_p q$$

Si

$$\rightarrow \mu_n = 1300 \text{ cm}^2/\text{V-s}$$

$$\mu_p = 500 \text{ cm}^2/\text{V-s}$$

$$\therefore \mu_n \approx 2 \mu_p$$

$$\therefore \mu_n \approx 2 \mu_p$$

$$\Rightarrow \sigma_n = 2 \sigma_p$$

$$\therefore R_p = 2 R_n$$

$$\therefore R_n = R \frac{S_n L}{A}$$

$$\downarrow R_p = \frac{S_p L}{A} \uparrow$$

$$\therefore R_p = 2 R_n$$

for  $R_p = R_n$

$$\therefore A_p = 2 A_n$$

$$\Rightarrow \left( \frac{W}{L} \right)_p = 2 \left( \frac{W}{L} \right)_n$$

⇒ nMOS

$$L = 1 \mu m$$

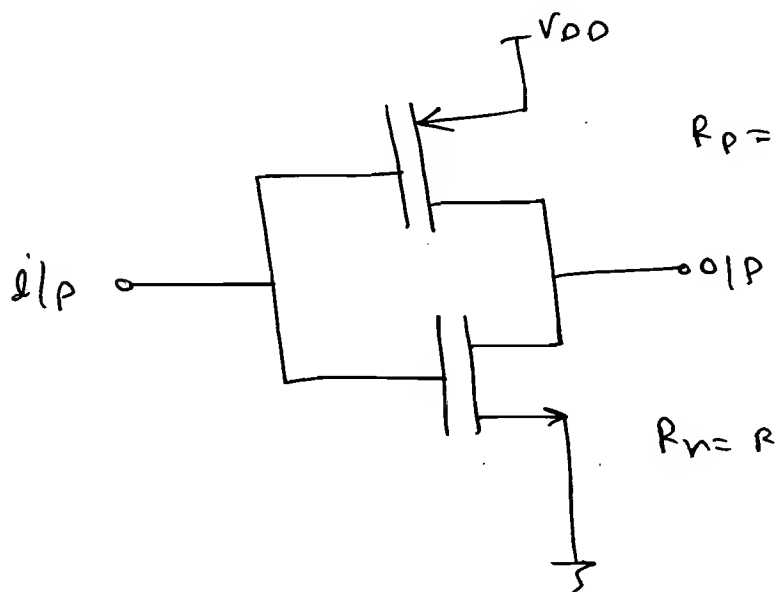
$$W = 1 \mu m$$

pMOS

$$L = 1 \mu m$$

$$W = 2 \mu m$$

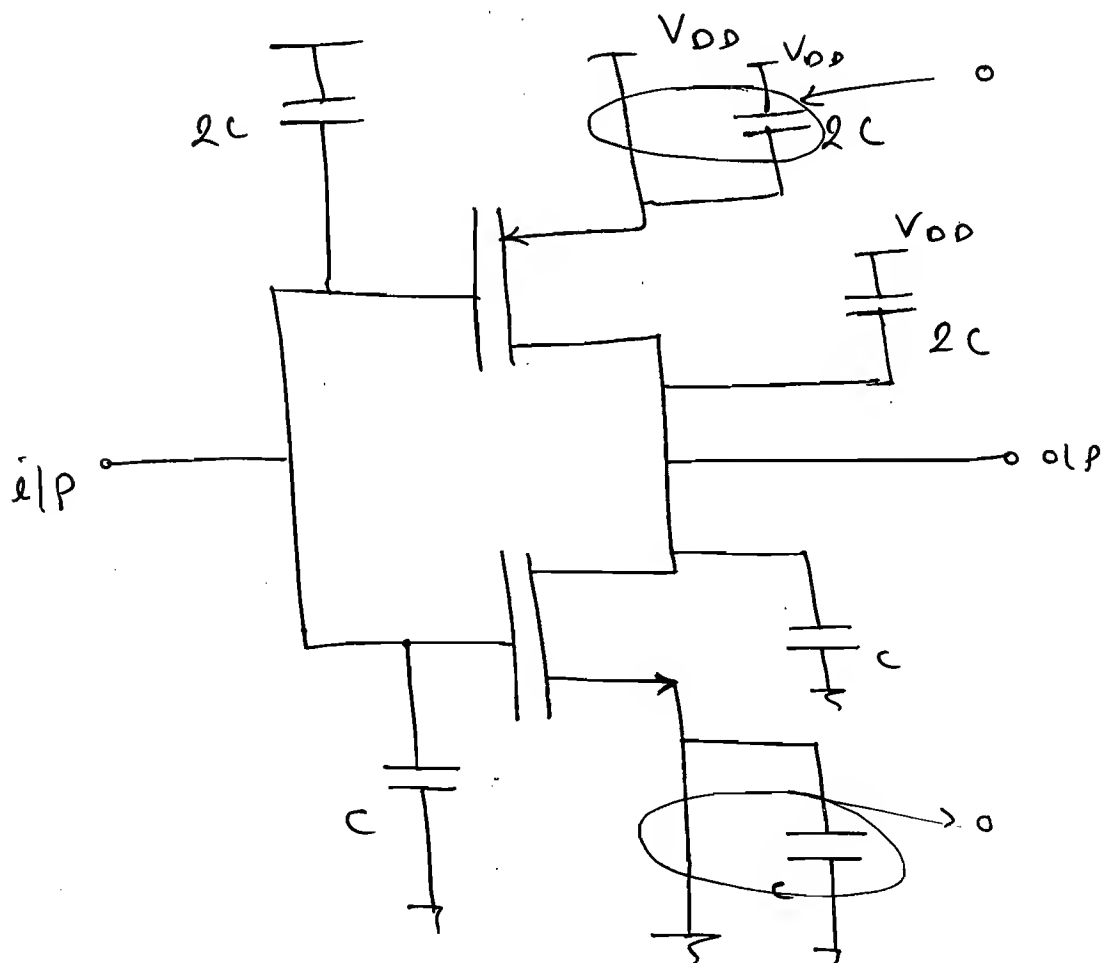
\*



$$R_p = \frac{2R}{2} = R.$$

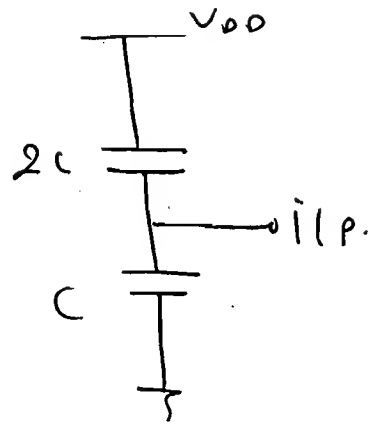
$$R \propto \frac{1}{(W/L)}$$

\*

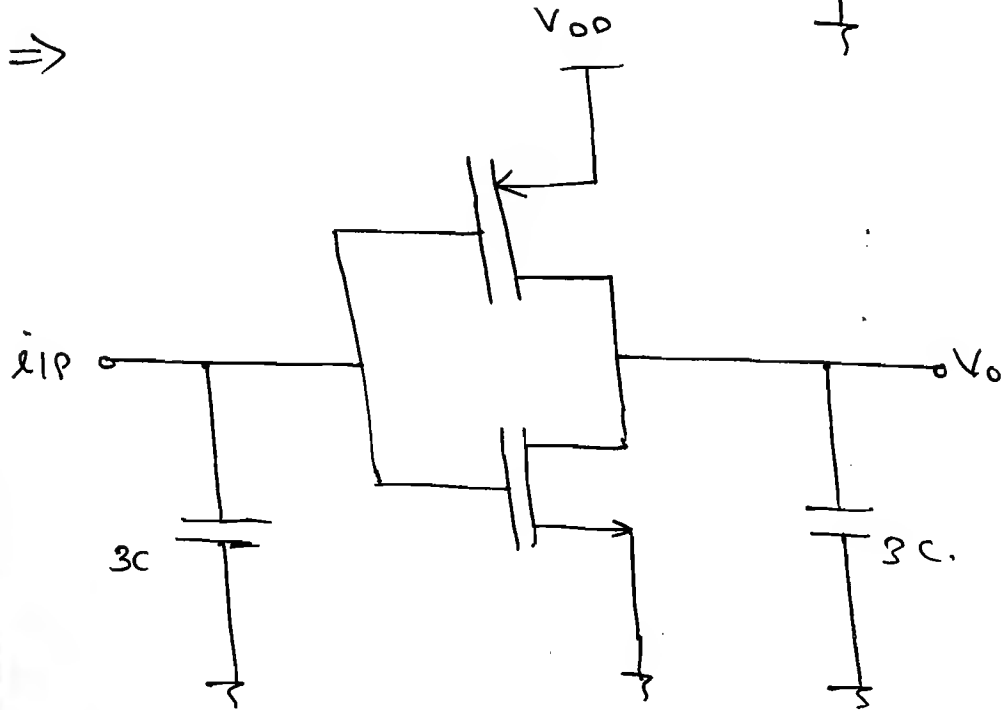


$$(C \propto \frac{WL}{L})$$

$\Rightarrow$  i/p capacitance,



$\Rightarrow$

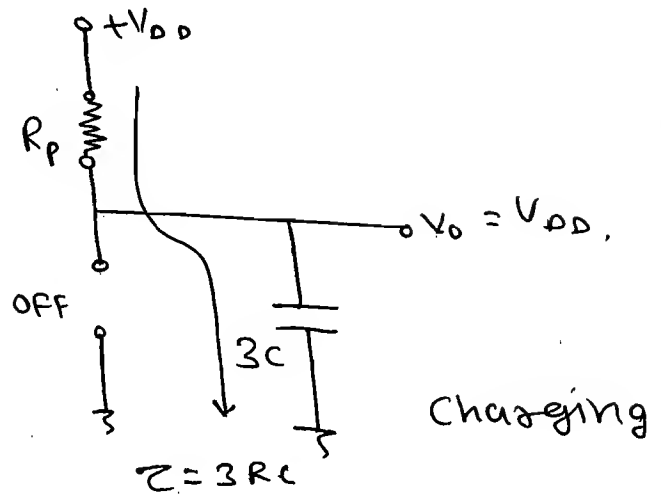


$\Rightarrow$  ①  $V_i = 0$

$\Rightarrow$  NMOS : OFF

$\Rightarrow$  PMOS : ON

Rise time ( $t_{pdr}$ ) =  $3CR_p$

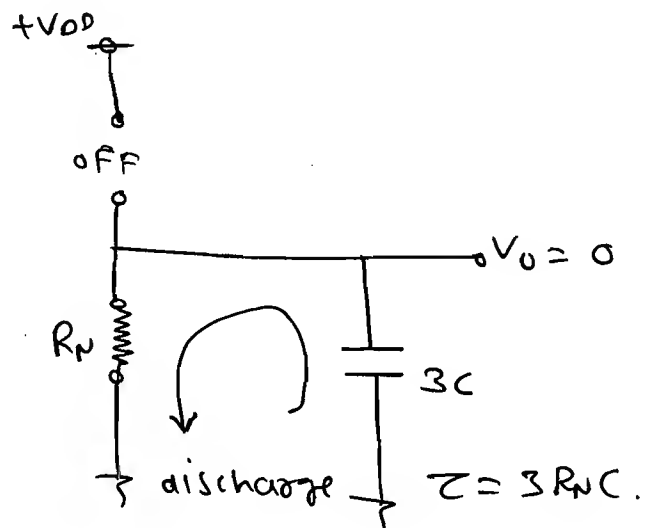


$\Rightarrow$  ②  $V_i = V_{DD}$

$\Rightarrow$  NMOS : ON

$\Rightarrow$  PMOS : OFF

Fall time ( $t_{pdf}$ ) =  $3R_n c$

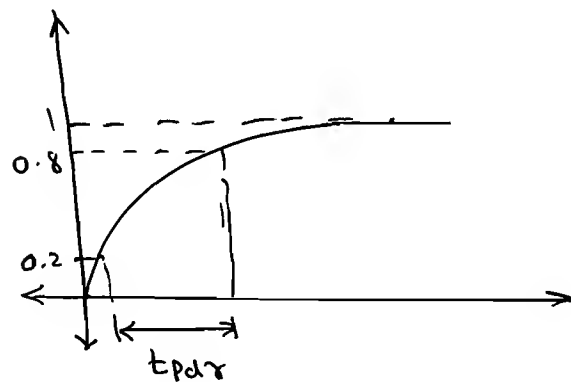


## \* Propagation Delay:

$$(t_{pd}) = \frac{t_{pdr} + t_{pdf}}{2}$$

## \* Rise-time ( $t_{pdr}$ ): ( $t_r$ )

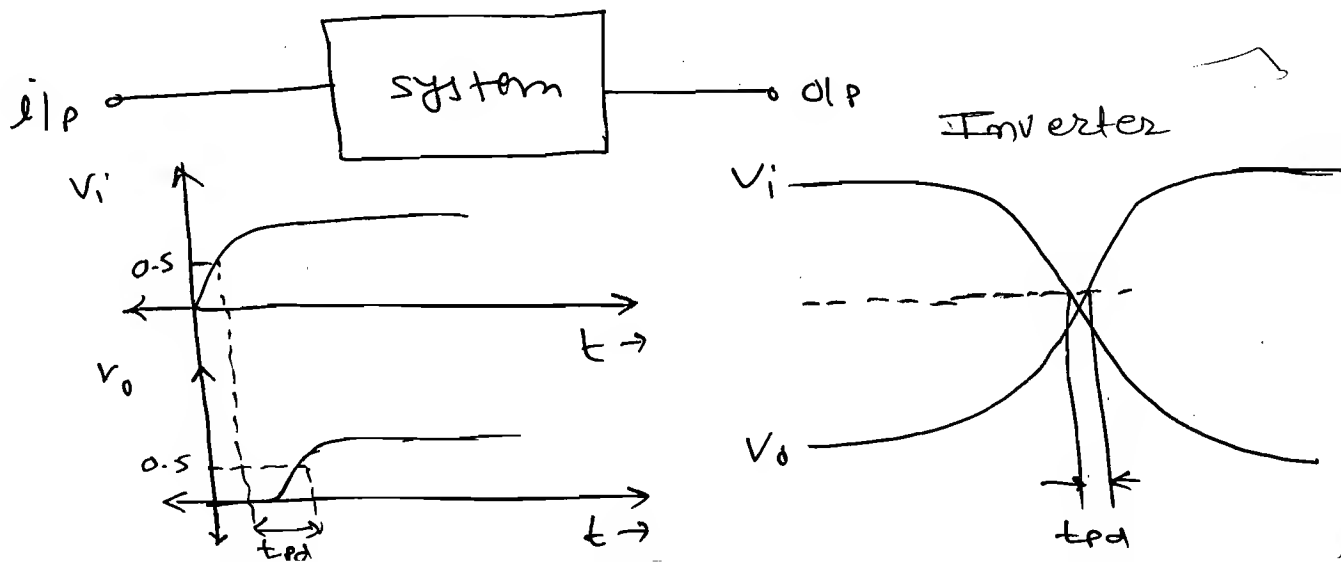
⇒ It is the time taken by the waveform to rise from 20% to 80% of its steady state value.



## ② Fall time ( $t_{f}$ ):

⇒ It is the time taken by the waveform to fall from 80% to 20% of its steady state value.

## ③ Propagation delay ( $t_{pd}$ ):



⇒ it is the max. time from the l/p crossing 50% to the o/p crossing 50%.

#### ④ Contamination Delay: ( $t_{cd}$ ):

⇒ It is the minimum time from the input crossing 50% to the o/p crossing 50%.

#### ☆ Power Calculation:

1. Dynamic Power
2. Static Power.

##### ① Dynamic Power:

⇒ Dynamic power is the power consumed by the MOSFET during its transition. i.e. it is the power consumed by the MOSFET during switching (or) Transition from Logic '1' to Logic '0' (or) from Logic '0' to Logic '1'.

(i) Capacitor Charging & discharging Power.

(ii) Short ckt Power & Crowbar Power.

##### (i) Capacitor Charging & Discharging Power:

⇒ The energy dissipated across the ~~Capacitor~~ P-mos transistor during capacitor charging,

$$E_c = \frac{1}{2} C \underbrace{V_{DD}^2}_{\text{total capacitance}}$$

⇒ The energy dissipated across the nmos transistor during discharging.

$$E_d = \frac{1}{2} C \cdot \underbrace{V_{DD}^2}_{\text{total capacitance}}$$

⇒ Total energy dissipated across pmos & nmos Transistors =  $E_d + E_c$

$$\therefore E = C V_{DD}^2$$

$$\therefore \text{Power } P = \frac{E}{T} = \frac{C V_{DD}^2}{T}$$

$$\therefore P = C V_{DD}^2 \cdot f$$

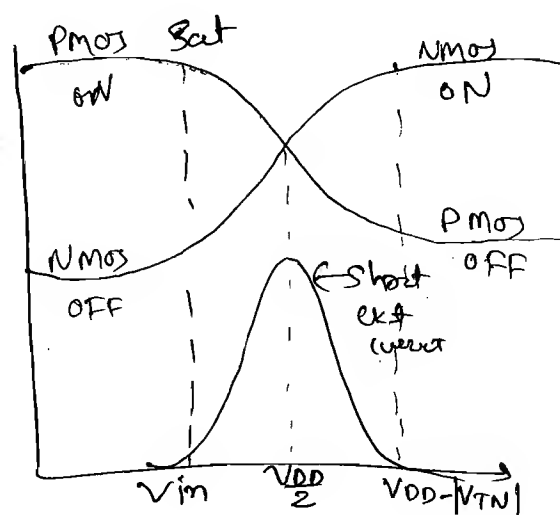
Time period  
freq<sup>n</sup> of switching

$$P_{\text{charge \& discharge}} = C V_{DD}^2 \cdot f$$

(ii) Short Ckt power:-

<u>Reg</u>	<u>Cond<sup>n</sup></u>	<u>Pmos</u>	<u>Nmos</u>
C	$V_i = \frac{V_{DD}}{2}$	Sat	Sat

$$P_{\text{short}}$$



⇒ Total Dynamic Power =  $P_{\text{charge \& discharge}} + P_{\text{short ckt}}$

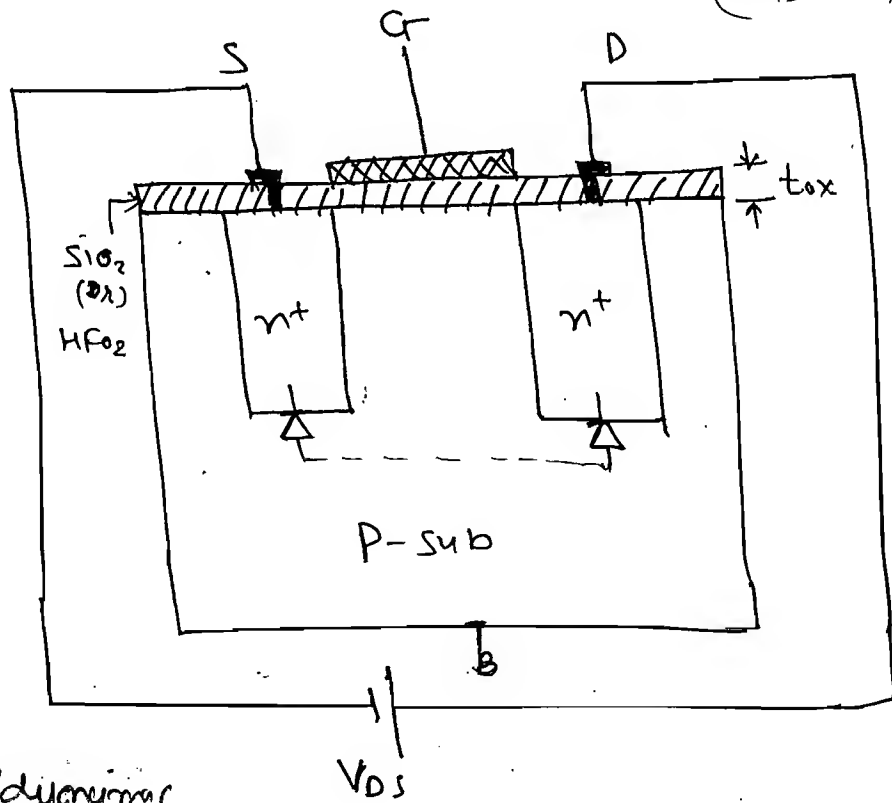
$$\approx P_{\text{charge \& discharge}}$$

$$P_{\text{dynamic}} = C V_{DD}^2 \cdot f$$

## (2.) Static Power:

⇒ Static power is the power consumed by the MOSFET during ideal state i.e. it is the power consumed by the MOSFET during continuously ON at Logic '1' state (or) continuously OFF at Logic '0' state. & this is due to

- (i) Gate oxide leakage current. ( $I_{g\text{leakage}}$ ).
- (ii) Junction leakage current. ( $I_{j\text{leakage}}$ ).
- (iii) Subthreshold leakage current. ( $I_{\text{subleak}}$ ).  
( $V_{GS} < V_T$ )



$$\epsilon_{\text{SiO}_2} = 3.9$$

$$\epsilon_{\text{HfO}_2} = 30.$$

up to  
90nm

$P_{\text{dym}} > P_{\text{stat}}$   
below 90nm

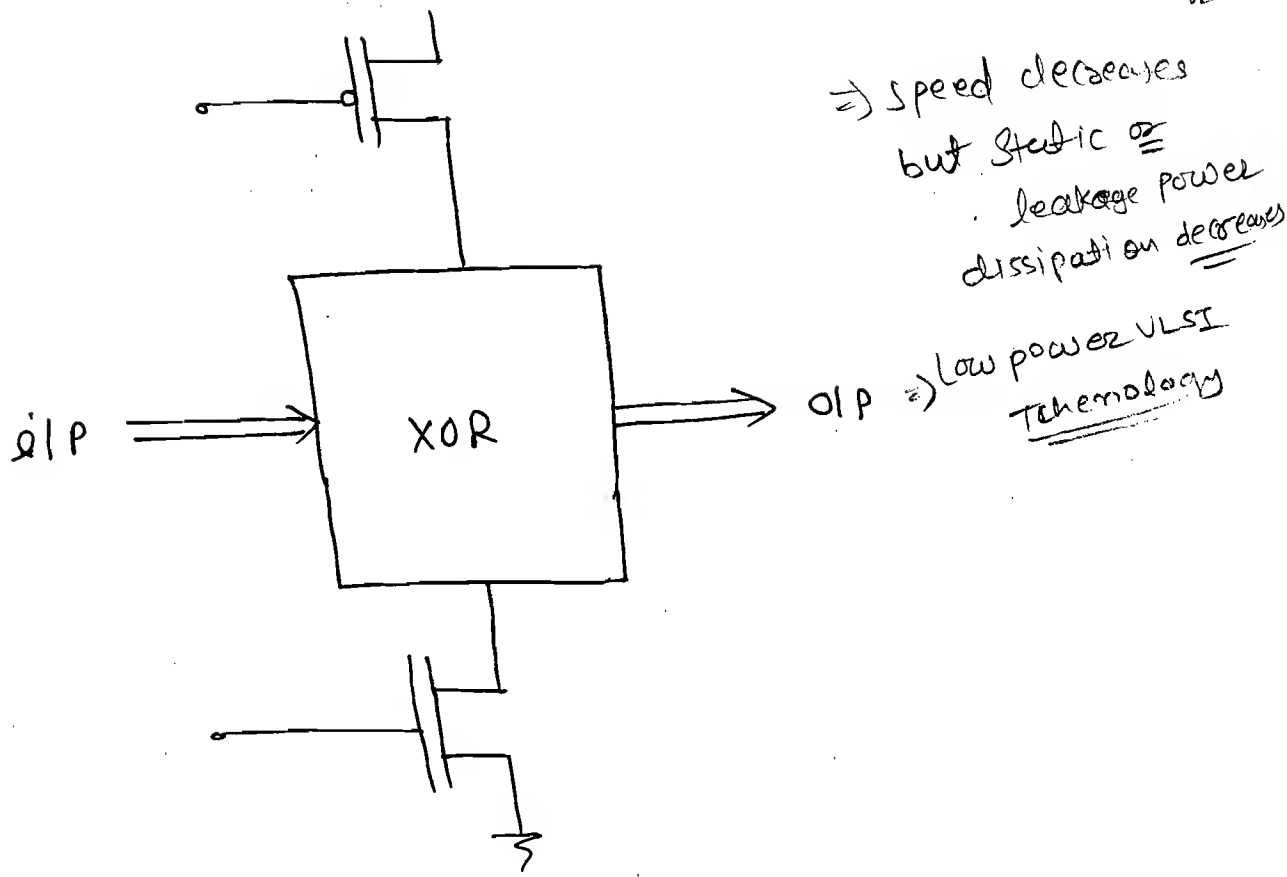
$P_{\text{static}} > P_{\text{dynamic}}$

$$\Rightarrow P_{\text{static}} = (I_{g\text{leak}} + I_{j\text{leak}} + I_{\text{subleak}}) V_{DD}.$$

∴

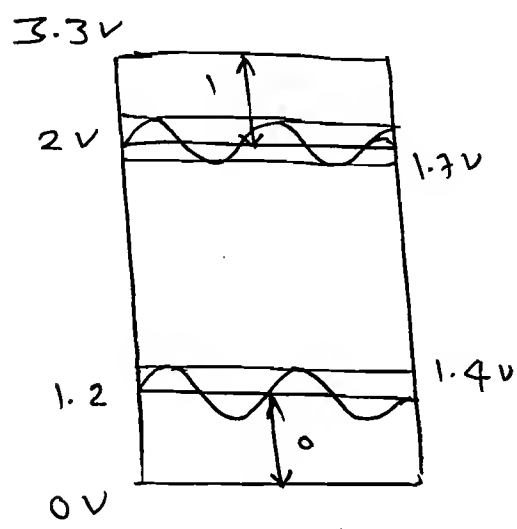
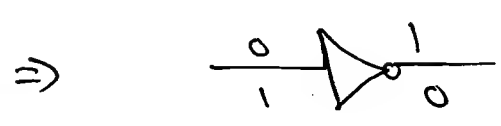
$$P = P_{\text{dynamic}} + P_{\text{static}}.$$





# \* Noise Margin:

⇒ Noise Margin allows you to determine maximum allowable noise voltage at the input of the gate without disturbing output.

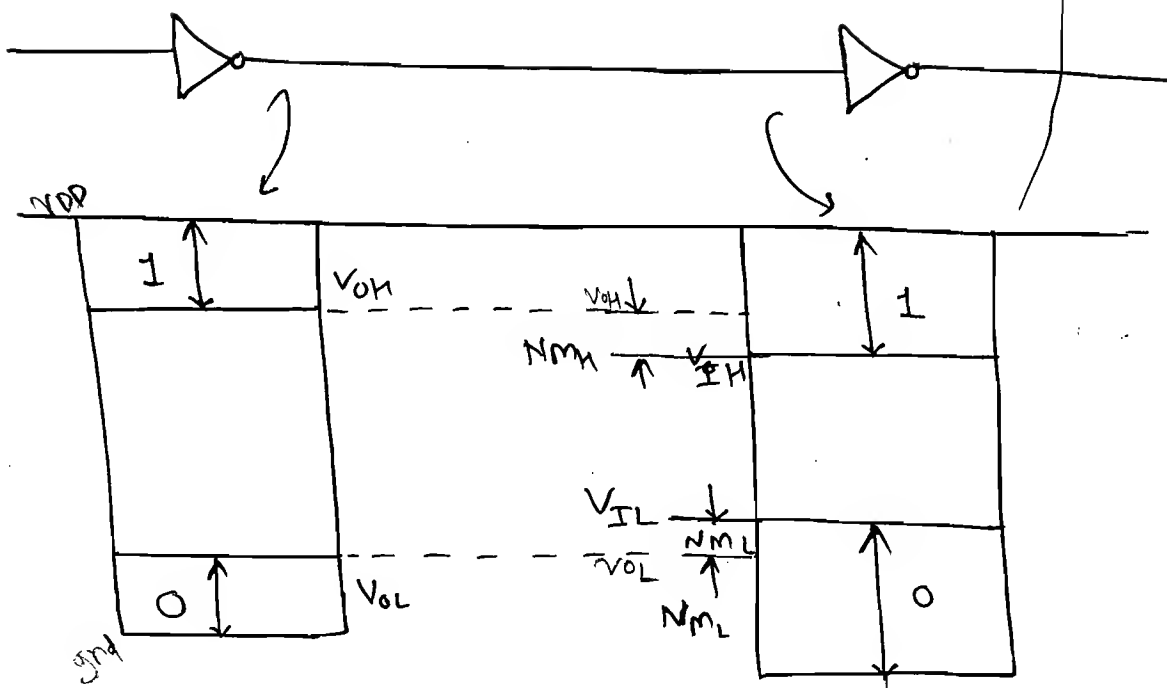


① High Noise Margin.  
( $NM_H$ ):

$$NM_H = V_{OH} - V_{IH}$$

② Low Noise Margin.  
( $NM_L$ ):

$$NM_L = V_{IL} - V_{OL}$$



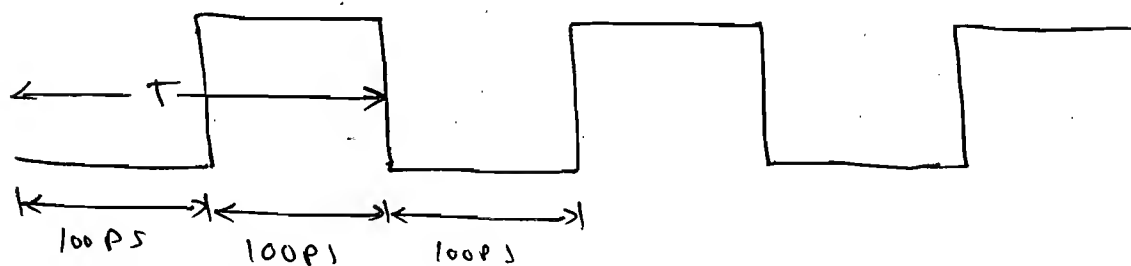
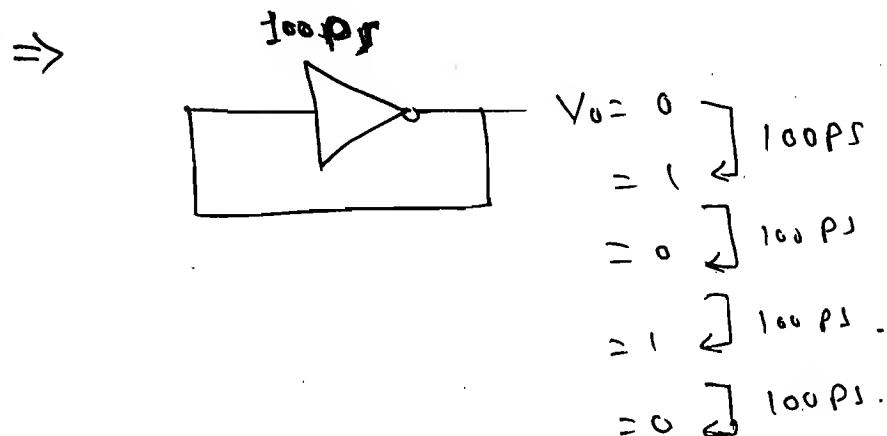
→  $V_{OH}$ : ~~max~~ Min. High o/p voltage.

$V_{IH}$ : ~~max~~ ~~high~~ min. High I/P voltage.

$V_{OL}$ : Max. Low o/p voltage.

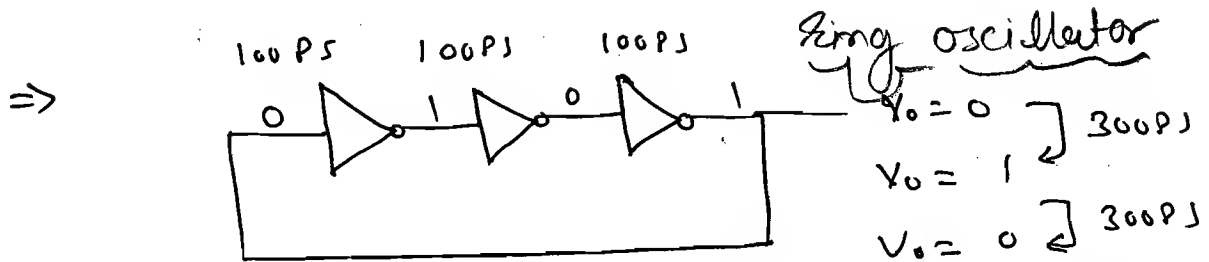
$V_{IL}$ : max. Low I/P voltage.

⇒ 
$$V_{OL} < V_{IL} < V_{IH} < V_{OH}.$$

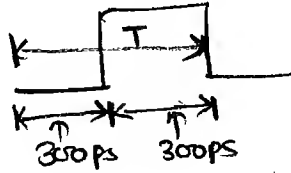


$$T = 200 \text{ pS}$$

$$f = \frac{1}{200 \text{ p}} \text{ Hz}$$



$$f_0 = \frac{1}{2Nn}$$



$$T = 600 \text{ pS}$$

$$f = \frac{1}{600 \text{ pS}}$$

$\Rightarrow N = \text{no. of inverters}$   
 $n = \text{delay of each inverter.}$

$$\therefore f_0 = \frac{1}{2 \times 3 \times 100} = \frac{1}{600 \text{ p}} \text{ Hz}$$

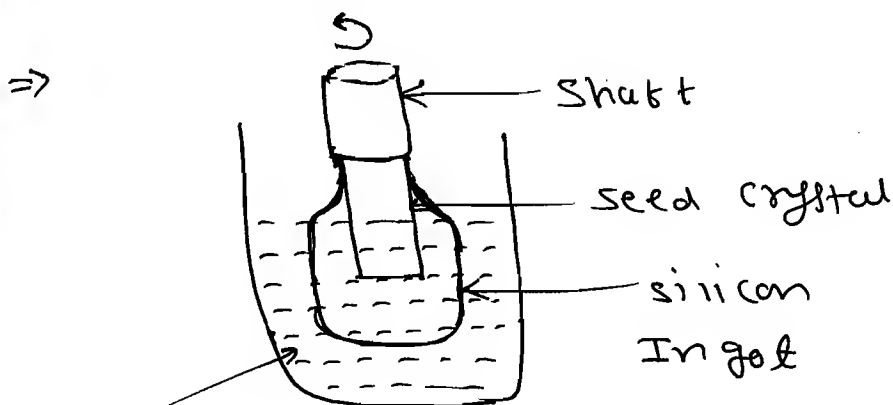
applicable only for  
 same time delay  
 for every inverter  
 & number of inverters  
 is odd

# ☆ Device Technology:

1. Crystal growth and wafer preparation.
2. Oxidation. ② → Epitaxy
3. Photolithography.
4. Diffusion.
5. Ion - Implantation.
6. Metallization.
7. Passivation.
8. Packing.

③ Crystal growth and wafer prep. Vacuum evaporation of aluminium

⇒ Czochralski Process:



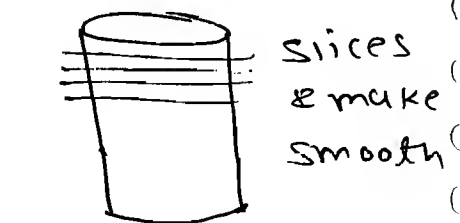
Impurity  
99.99999

1425°C

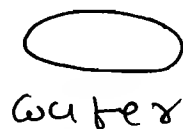
growth rate  
30-150mm/hour

100 cm → length

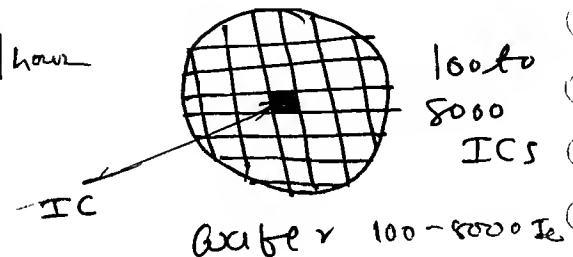
15 cm → Diameter



Silicon Ingot



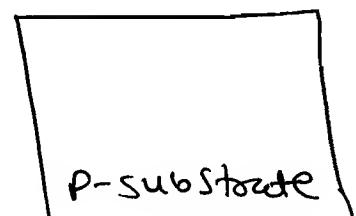
Wafer



⇒ Wafer thickness = 16 to 32 mil.

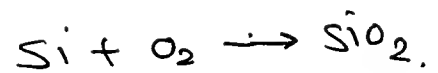
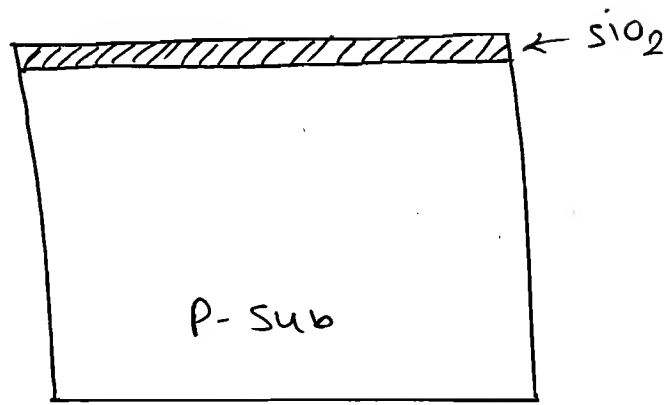
1 mil = 254μm

⇒ Diameter : 75 to 300mm.



p-substrate

## (2) Oxidation:



⇒ It is easy to form SiO<sub>2</sub> on top of the silicon without adding any extra material.

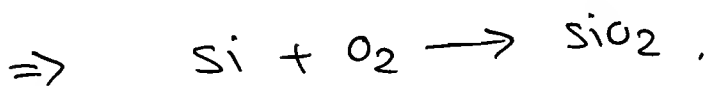
⇒ It doesn't allow any impurity through it.

⇒ It dissolves only in Hydrochloric Acid.

⇒ SiO<sub>2</sub> is a dielectric material; therefore it can be used as an insulator (or) isolator between two devices (or) two stages.

⇒ There are two methods of oxidation:

### ① Dry oxidation:



→ take place at 1200°C.

→ Slow process.

→ Thin layers.

→ Dry oxidation is a slow process. But

the electric properties of Dry oxidation is better than wet oxidation.

(ii) Wet oxidation:

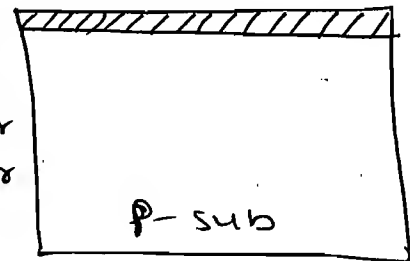


→ 900° to 1000°C

→ Fast

→ thick layers.

1mm  $\updownarrow$   
1hr  
2mm 3hr  
4mm 8hr



(iii) Photolithography:

⇒ Photo → ~~picture~~ lights

Lithos → Stone

graphy → picture.

→ (i) Photoresist ✓

(ii) Photo mask. ✓

(iii) UV rays. ✓

(iv) Developing. ✓

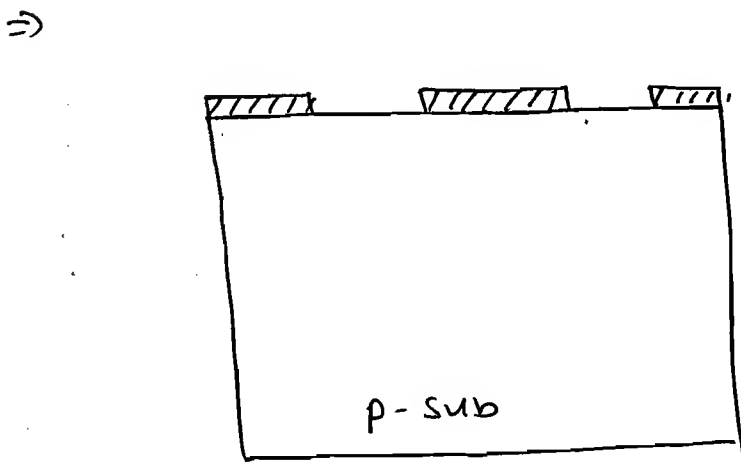
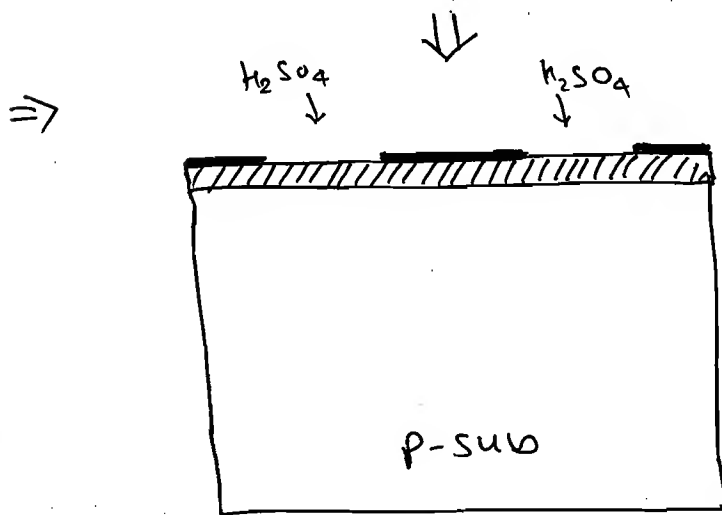
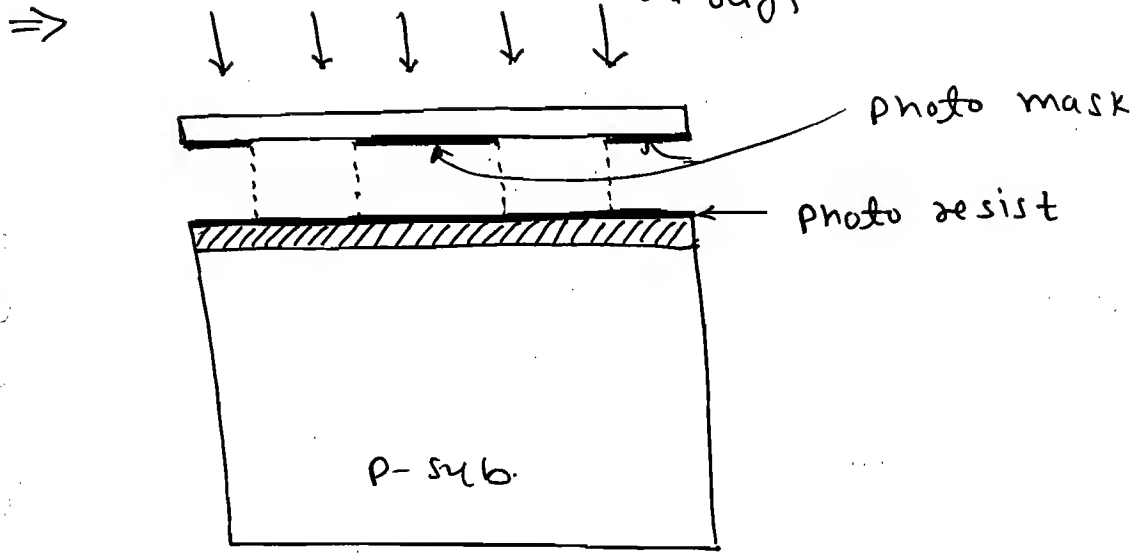
(v) Etching. ✓

(vi) Stripping. ✓

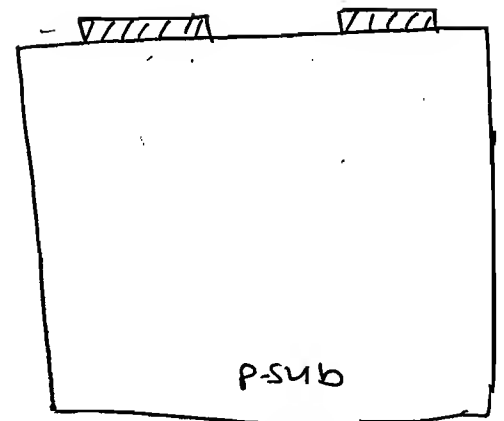
⇒ Stripping is a process of removing unwanted portion.

⇒ photo resist:

① positive photo resist ② Negative photo resist.



positive photo resist

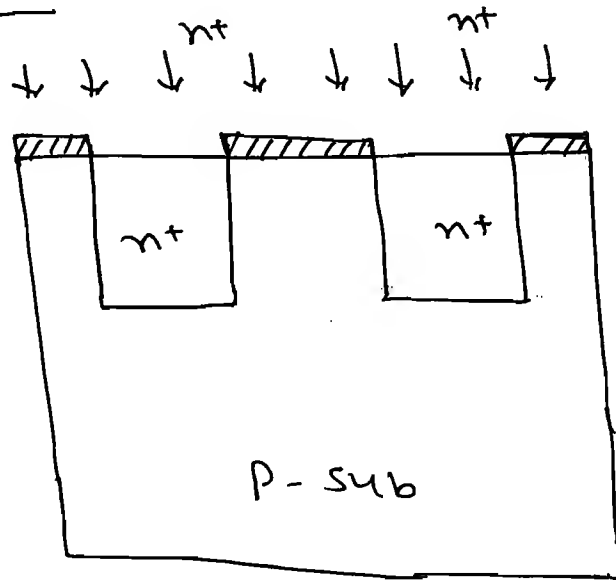


negative photo resist.

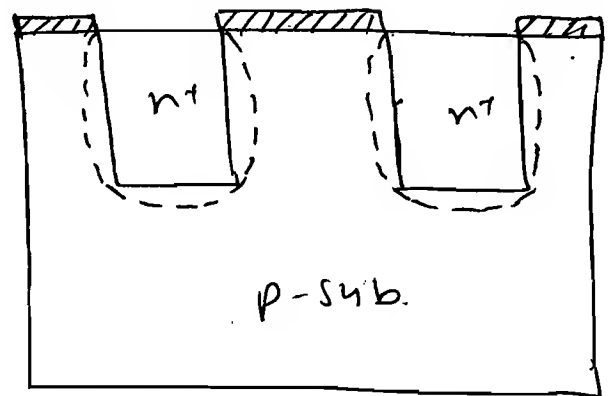
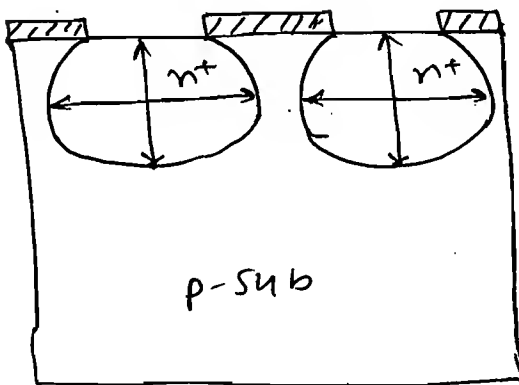
⇒ The portion of the silicon dioxide which is exposed to uv rays it gets removed during etching process then it is called positive photo resist.

⇒ The portion of the silicon dioxide which is not exposed to UV rays if it gets removed during etching then it is called -ve photo resist.

#### (4) Diffusion:



(i) Isotropic diffusion: (ii) Anisotropic diffusion:



⇒ Take Place:  $1000^{\circ}\text{C}$

⇒ for  $n^+$  type:  $\text{P}_2\text{O}_5$ ,  $\text{POCl}_3$  (Phosphorus oxide chloride).

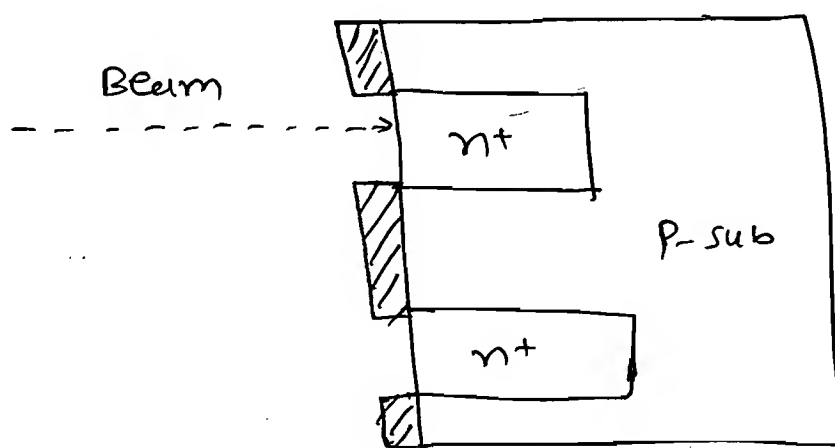
⇒ for  $p^+$  type:  $\text{BrO}_3$ ,  $\text{BCl}_3$ .  
(S & D)



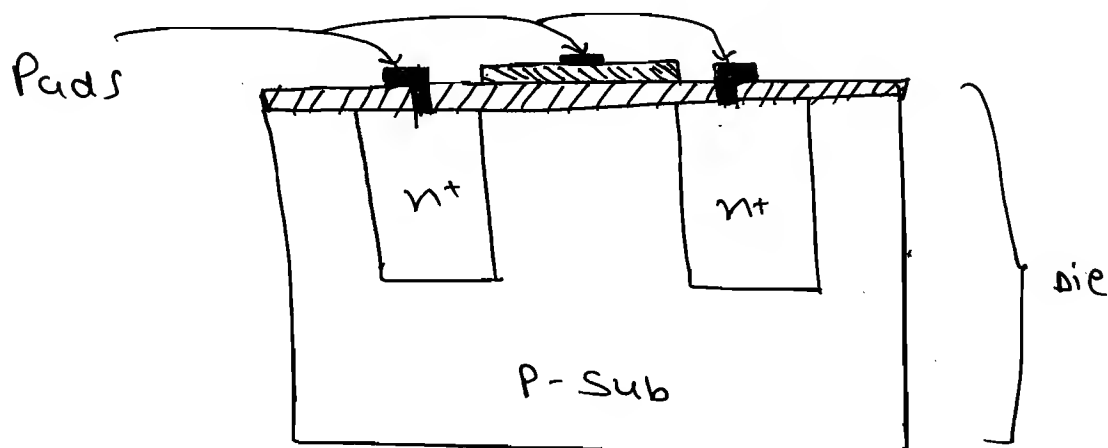
## (5) Ion - Implementation:

⇒ It is also same as diffusion process but it takes place at lower temperature and slow process.

⇒



## (6) Metallization:



⇒ Metallization is a process of forming metallic contact between the device for interconnection.

⇒ old design: Al

⇒ New design: Cu

( $\sigma_{Cu} > \sigma_{Al}$ ) ⇒ to reduce contact resistance.

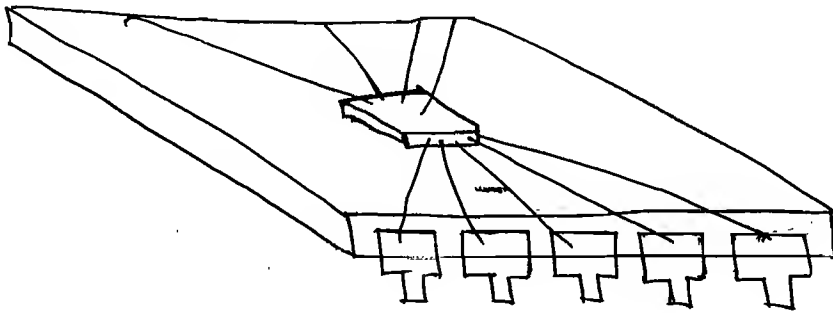
## (7.) Passivation:

⇒ Passivation is a process of forming glass type or epoxy coating on the surface of the die to protect it from the atmosphere and also to provide mechanical strength.

## (8) Packing:

Die: 10 to 20%.

⇒



→ more than 200 types of packing.

→ DIP package.

→ PLCC, QFN

→ PGA (pin grid array).

→ BGA (Ball grid array)

↑  
Low Power like memories, MP.

